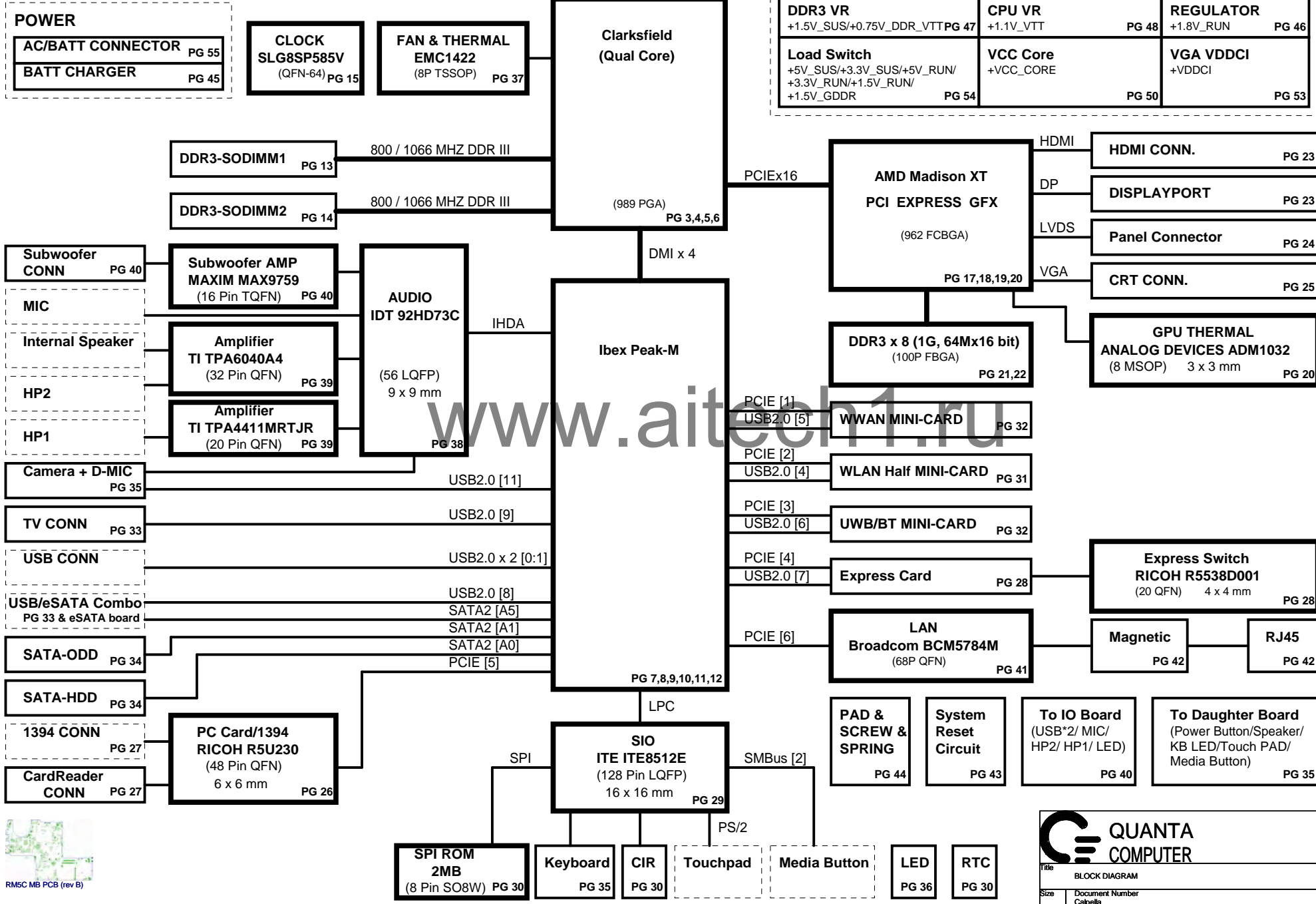


PWA :  
PWB : Y509R  
SCH : Y510R

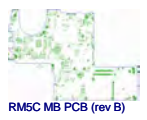
# Calpella Intel Discrete Block Diagram

VER : B1B



## SYSTEM POWER

<b>PCH REGULATOR</b> +1.05V_PCH PG 49	<b>SYS VR</b> +5V_ALW2/+3.3V_ALW +5V_ALW/+15V_ALW PG 51	<b>VGA Core</b> +VCC_GFX_CORE +1.1V_GFX_PCIE PG 52
<b>DDR3 VR</b> +1.5V_SUS/+0.75V_DDR_VTT PG 47	<b>CPU VR</b> +1.1V_VTT PG 48	<b>REGULATOR</b> +1.8V_RUN PG 46
<b>Load Switch</b> +5V_SUS/+3.3V_SUS/+5V_RUN/ +3.3V_RUN/+1.5V_RUN/ +1.5V_GDDR PG 54	<b>VCC Core</b> +VCC_CORE PG 50	<b>VGA VDDCI</b> +VDDCI PG 53



Title: BLOCK DIAGRAM

Size: Document Number: Calpella

Date: Friday, October 23, 2009

Sheet: 1 of 60





Rev: B1B

Table of Contents

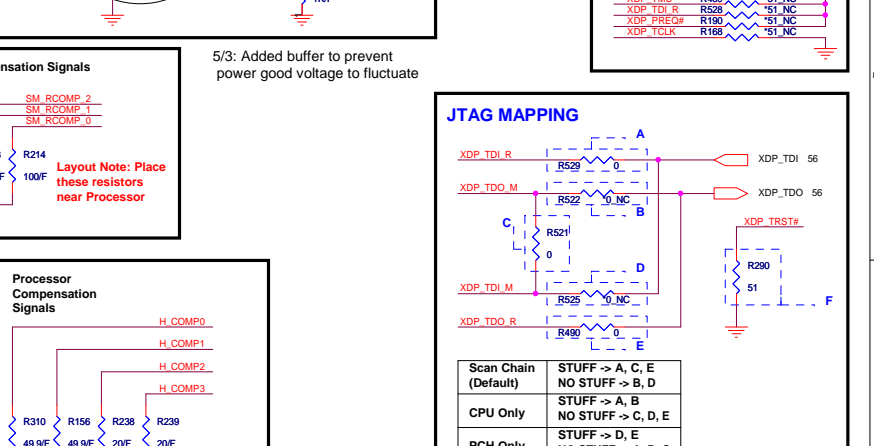
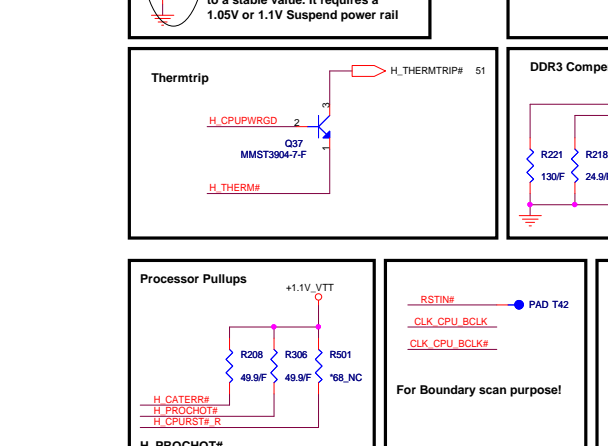
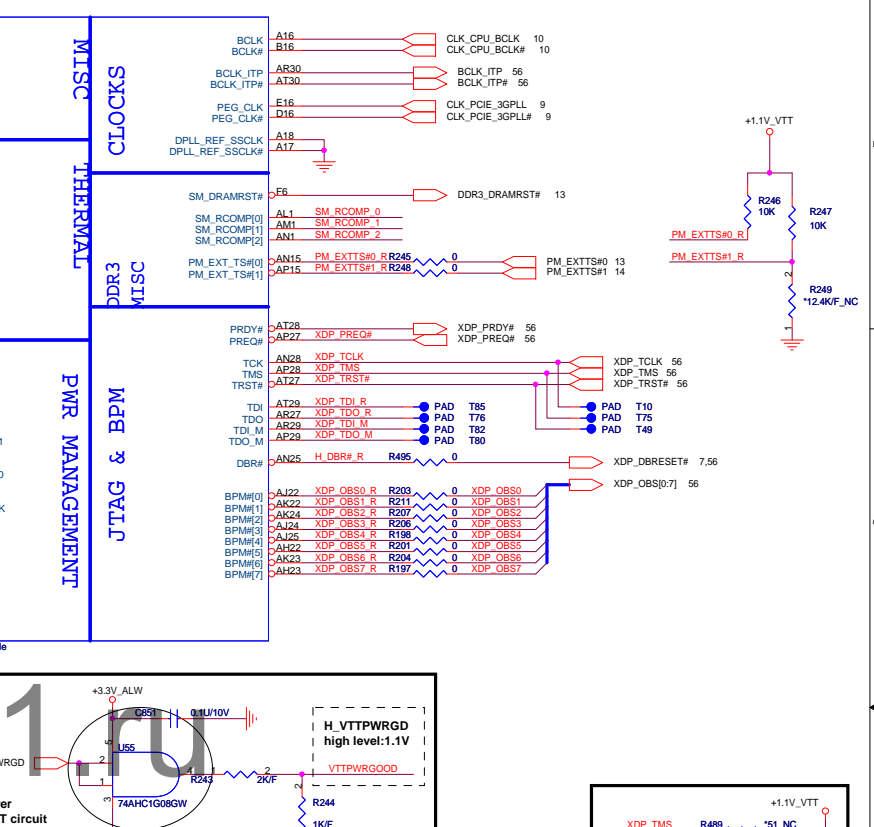
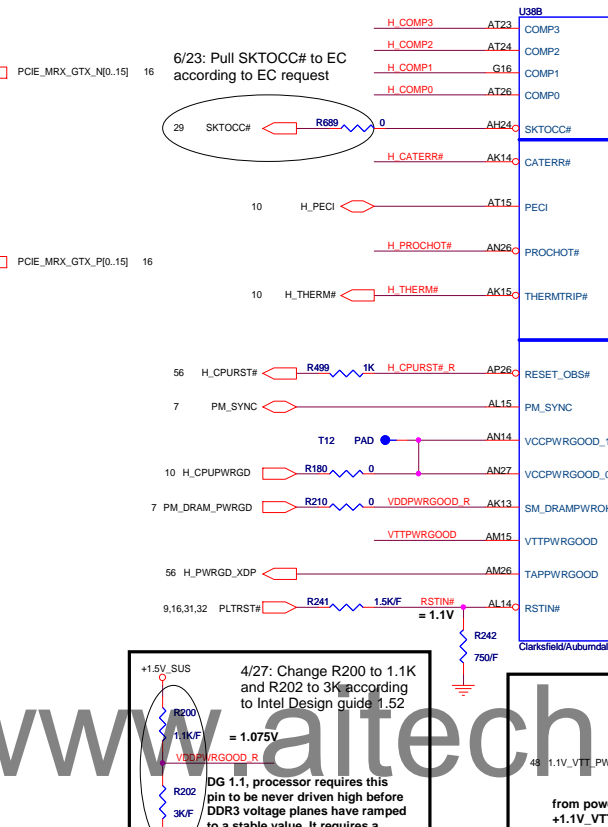
PAGE	DESCRIPTION
1	Block Diagram
2	Front Page
3-6	CPU (Clarksfield)
7-12	PCH (IBex Peak-M)
13-14	DDR3 SO-DIMM(204P)
15	Clock Generator
16-22	GPU (M96XT)
23	HDMI & DP
24	LCD connector
25	CRT
26	Card reader PCIe interface
27	Card reader & 1394 CONN
28	Express card
29	SIO (IT8512)
30	Flash/RTC/CIR
31	WLAN
32	WWAN/WPAN
33	USB & eSATA & TV
34	SATA HDD & ODD
35	KB/CCD/UI
36	LED
37	FAN/Thermal
38-40	Audio/CONN/Subwoofer (92HD73C).
41-42	LAN/RJ45 (BCM5784M)
43	System Reset Circuit
44	PAD & SCREW & SPRING
45	CHARGER (MAX8731A)
46	1.8V_RUN (TPS51218)
47	1.5_SUS/0.75(TPS51116)
48	1.1V_VTT(TPS51218)
49	1.05V_PCH (TPS51218)
50	VCC_CORE(MAX17036GTL+)
51	3.3V/5V/15V (MAX17020)
52	VGA_M97(MAX8792)
53	VDDCI_M97(TPS51218)
54	Run Power Switch
55	DCIN & Batt
56	XDP Connector
57	Power Block Diagram
58	SMBUS BLOCK
59	Power status

Power States

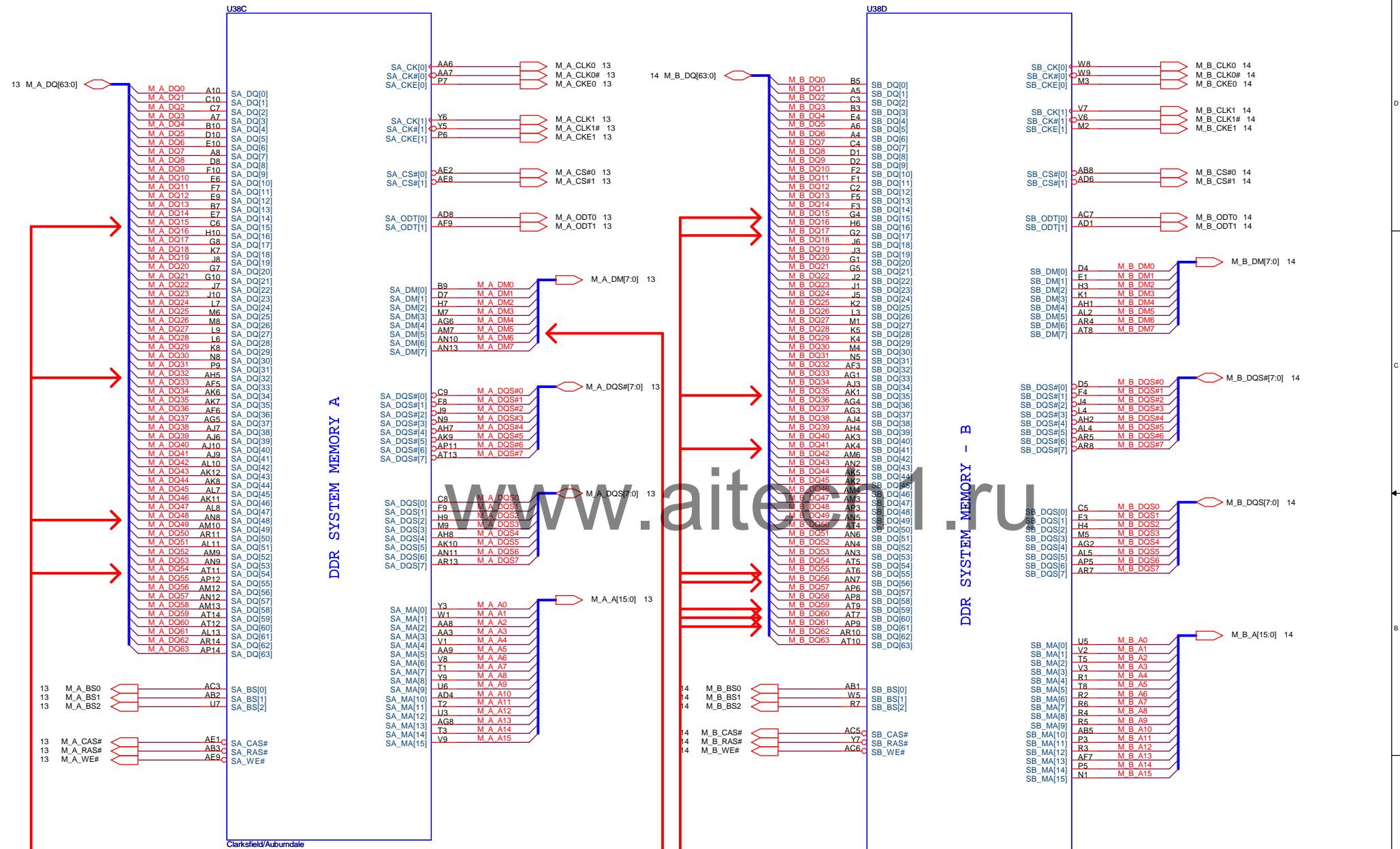
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51,52,53	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	8,11,29,30	RTC		S0~S5
+3.3V_ALW	+3.3V	3,29,30,34,35,36,43,45,51,54,55	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	24,33,34,35,47,51,52,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	24,34,51,54	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	41,42	LAN POWER	AUX_ON	
+5V_SUS	+5V	11,46,48,49,52,53,54	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	7,8,9,10,11,20,24,28,29,42,43,46,47,48,49,52,53,54	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.5V_SUS	+1.5V	3,5,13,14,47,52,54	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,54	SODIMM POWER	SUS_ON	
+5V_RUN	+5V	11,18,23,25,33,35,36,37,38,50,54	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	7,8,9,10,11,13,14,15,18,23,24,26,28,29,30,31,32,33,34,35,36,37,38,39,40,41,50,52,54,56	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	5,11,17,18,19,46,54	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	28,31,32,54	PCH POWER	1.5V_RUN_ON	
+1.1V_VTT	+1.1V	3,5,10,11,48,50,56	CPU POWER	RUN_ON	
+1.05V_PCH	+1.05V	8,9,11,15,49	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.5V	5,50	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	34	Module Power	MODC_EN#	
+5V_HDD	+5V	34	HDD Power	HDDC_EN#	
+5V_ALW2	+5V	35,36,51,54,55	LED power source	LDO output	

GND PLANE	PAGE	DESCRIPTION
 AGND	38,39,40	
 AGND_DC/DC	51	
 AGND_VCORE	50	
 GND	ALL	

## AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]  
Requires minimum 12mils spacing  
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]  
Requires minimum 12mils spacing  
with all other signals, including data signals.

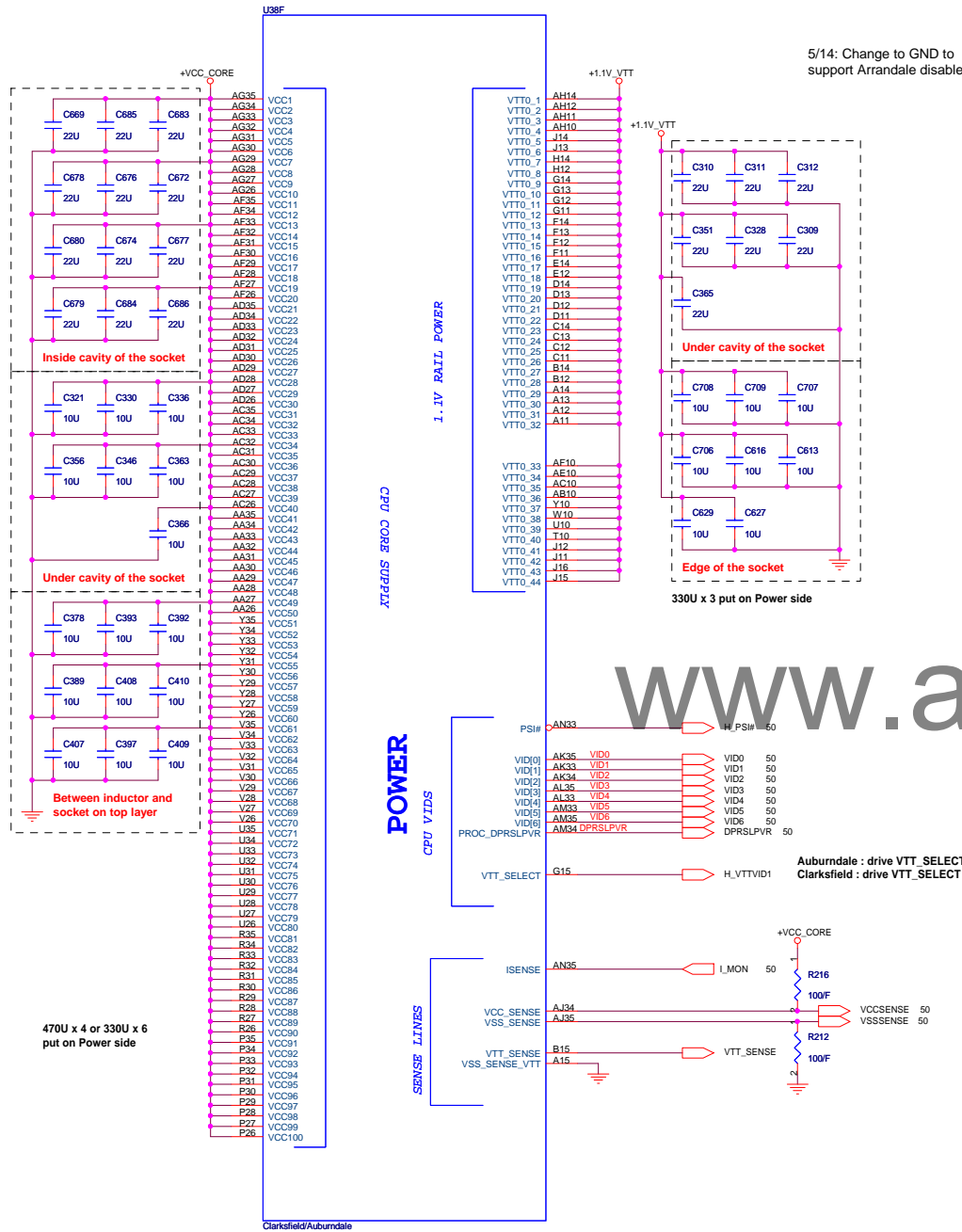
**QUANTA  
COMPUTER**

Title CPU 24(DDR)		
Size	Document Number RMSC	Rev B1B
Date:	Friday, October 23, 2009	Sheet 4 of 60

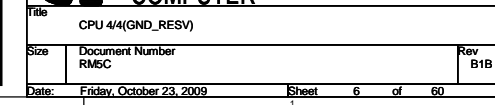


# AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

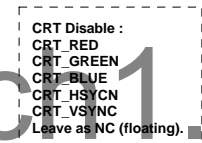
# AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



**AUBURNDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)**



### IBEX PEAK-M (LVDS,DDI)



Title PCH 1/6(DMI\_VIDEO)

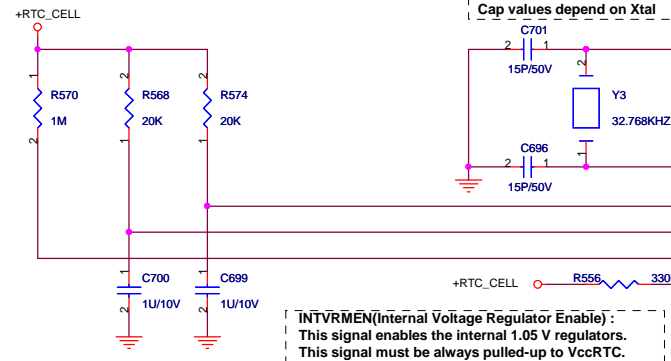
Size	Document Number BM5C
------	-------------------------

Date: Friday, October 23, 2009

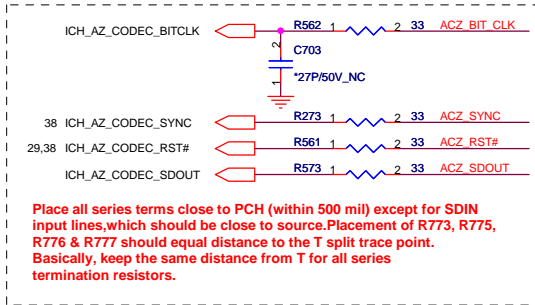
Rev  
B1

Sheet 7 of 60

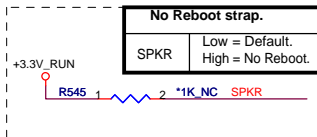
# IBEX PEAK-M (HDA,JTAG,SATA)



**INTVRMEN (Internal Voltage Regulator Enable):**  
This signal enables the internal 1.05 V regulators.  
This signal must be always pulled-up to VccRTC.



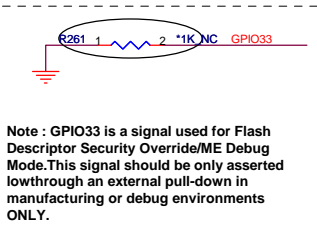
Place all series terms close to PCH (within 500 mil) except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.



**No Reboot strap.**

Low = Default.  
High = No Reboot.

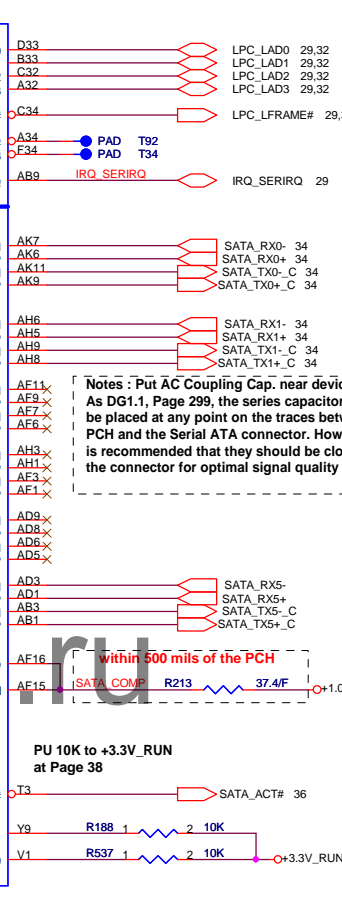
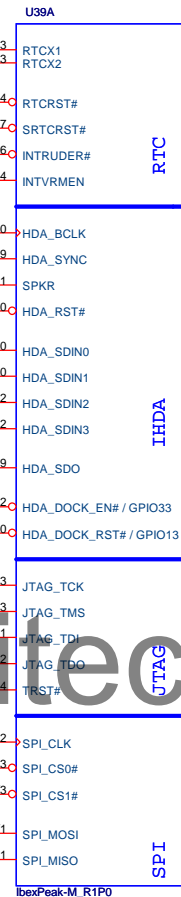
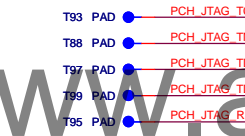
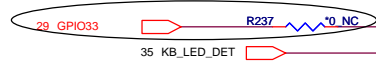
Scott\_0630: Change R545 footprint from RC0402-C to RC0402.



**Note:** GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode. This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.

6/2: Change R261 from 10K\_NC to 1K\_NC according to Intel design guide 1.51

1007 for change list

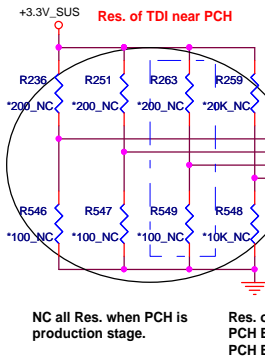


**Notes:** Put AC Coupling Cap. near device side. As DG1.1, Page 299, the series capacitors may be placed at any point on the traces between PCH and the Serial ATA connector. However, it is recommended that they should be close to the connector for optimal signal quality

**Notes:** FIS-based Port Multiplier support on SATA Ports 4 and 5 in AHCI/RAID mode.

PU 10K to +3.3V\_RUN at Page 38

6/2: NC JTAG resistors as PCH is in QT stage



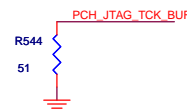
**Res. of TDI near PCH**

Scott\_0707: Reserve PCH\_JTAG\_RST# circuit as review.

NC all Res. when PCH is production stage.  
Res. of TDO PCH ES1 stage: NC  
PCH ES2 stage: pop

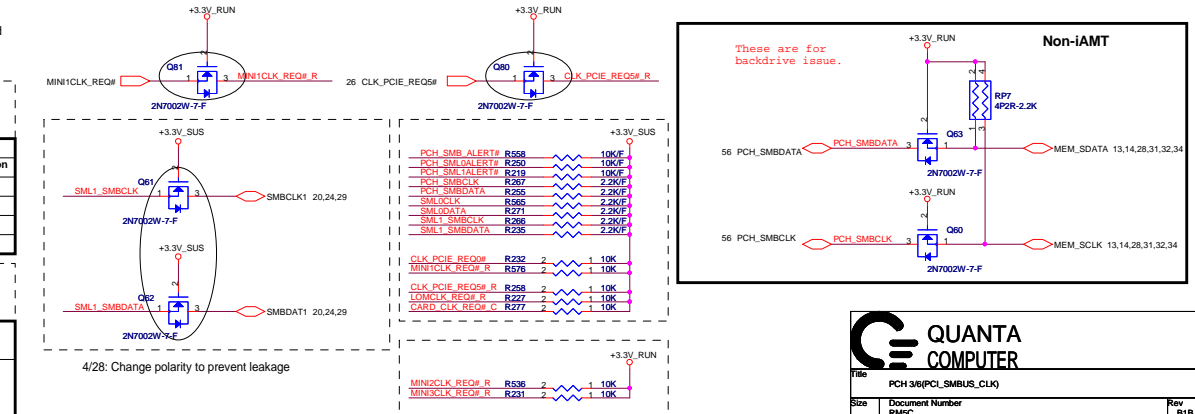
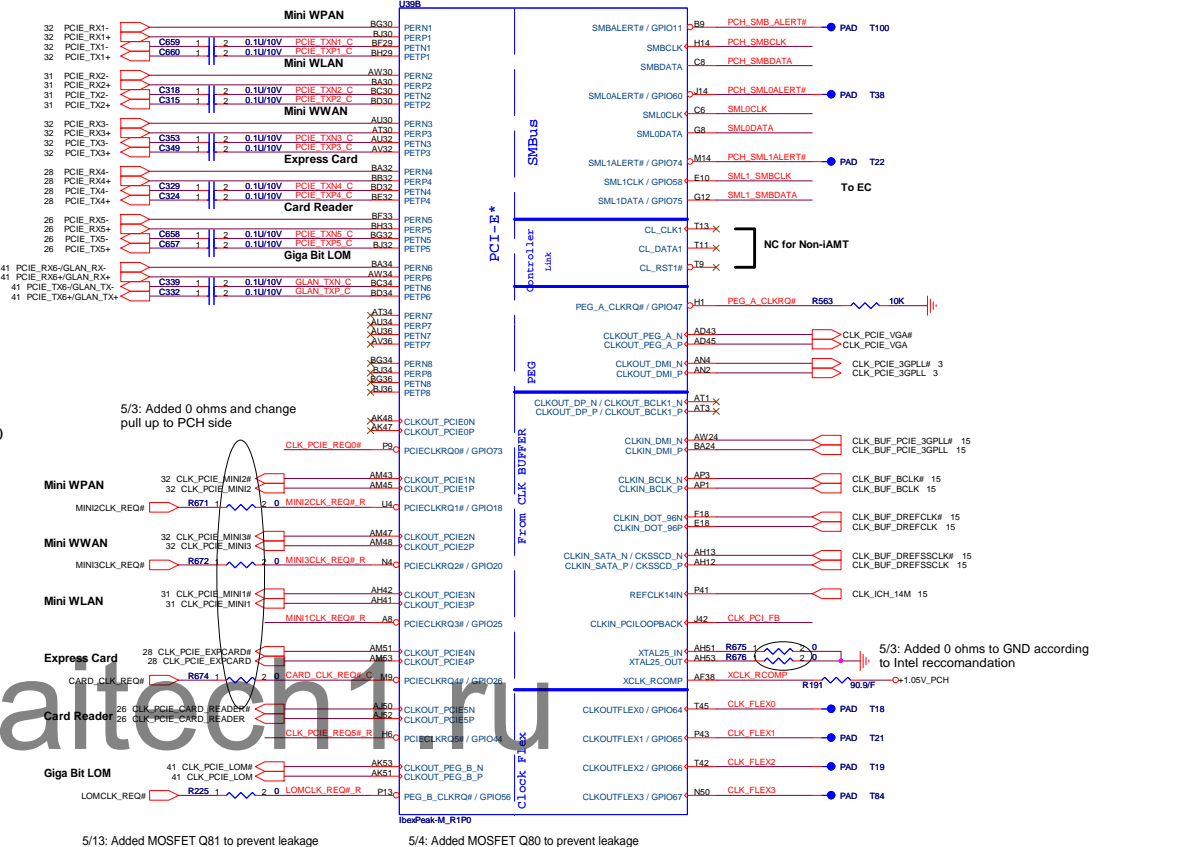
**Note:** Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

Scott\_0703: Note: Delete pull up 1.05V according to Intel change notice! (Reserved for debug purpose)



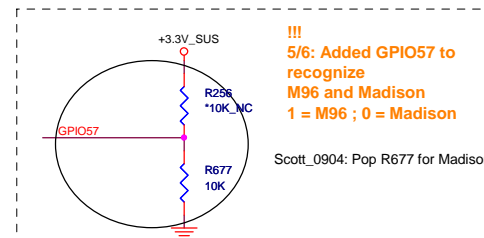
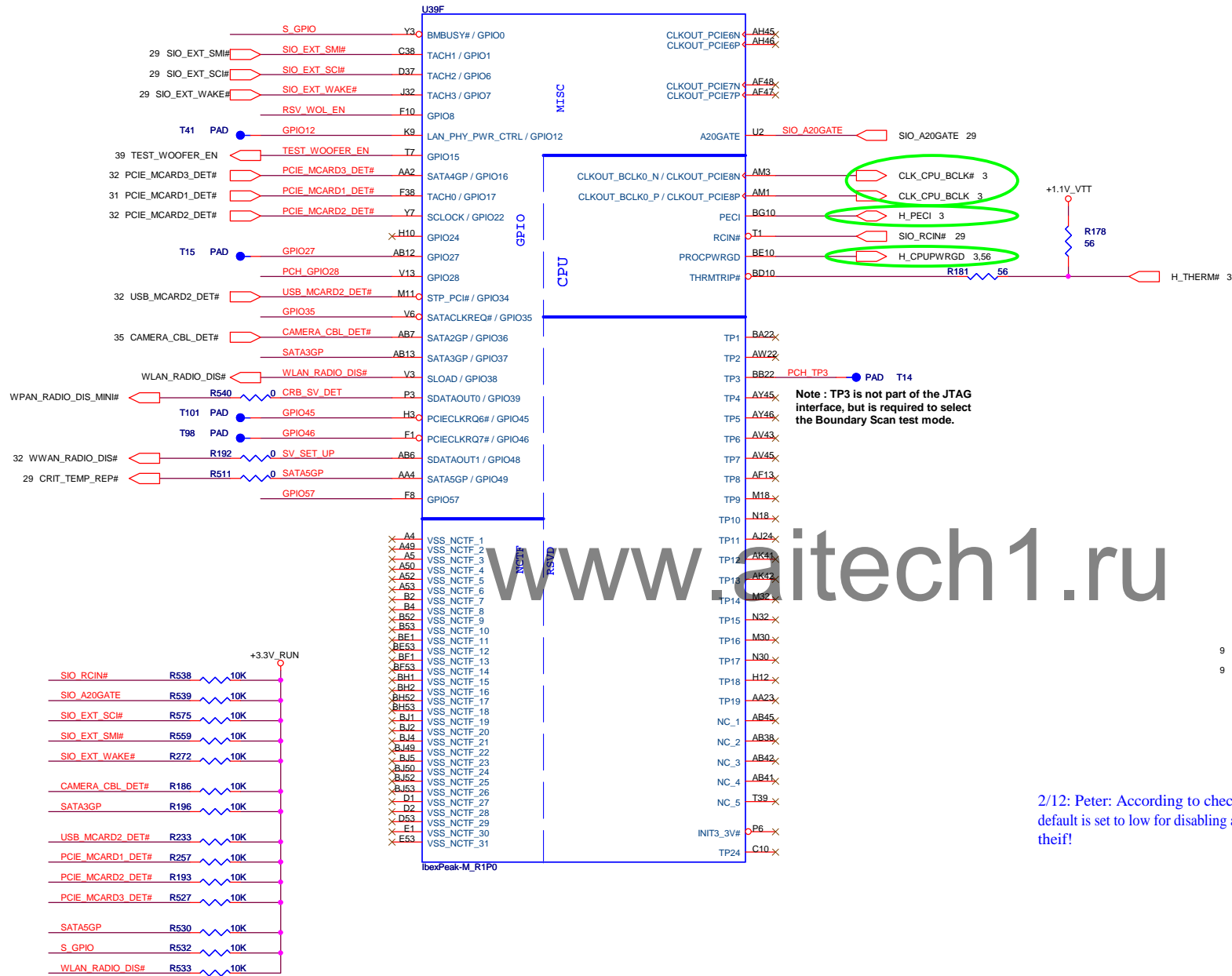
Title			
PCH 2/6(SATA_SPI)			
Size	Document Number		Rev
	RM5C		
Date:	Friday, October 23, 2009	Sheet	8 of 60

## IBEX PEAK-M (PCI-E,SMBUS,CLK)



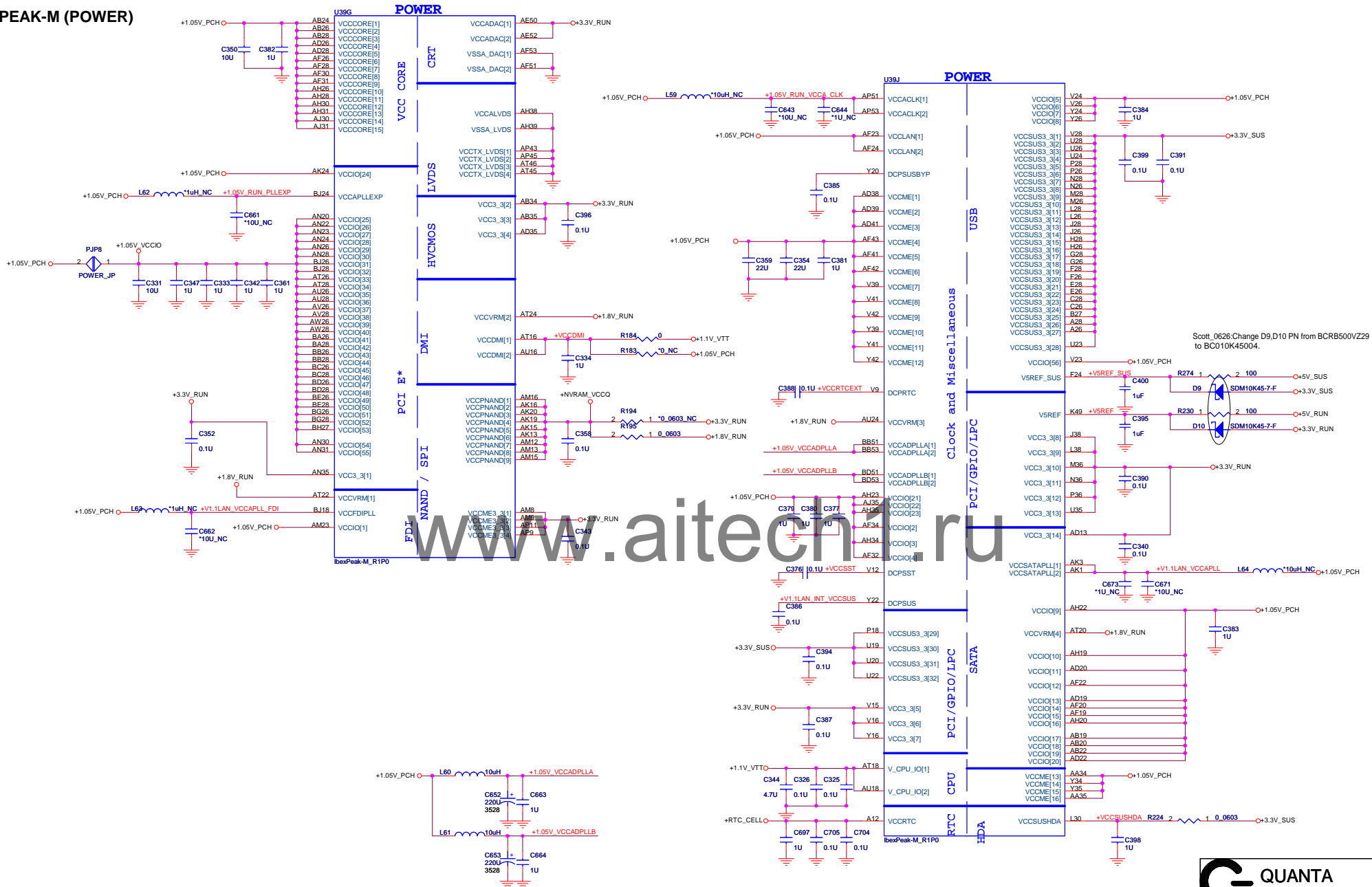


# IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)





### IBEX PEAK-M (POWER)



**Use External Graphics. Can connect power directly without Inductor & Cap ? As Ibex peak-M EDS 1.0, need +1.05V. Can use +1.1V\_VTT as CPU ?**



Title PCH 5/6(POWER)

Size	Document Number RM5C
------	-------------------------

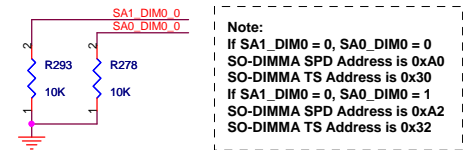
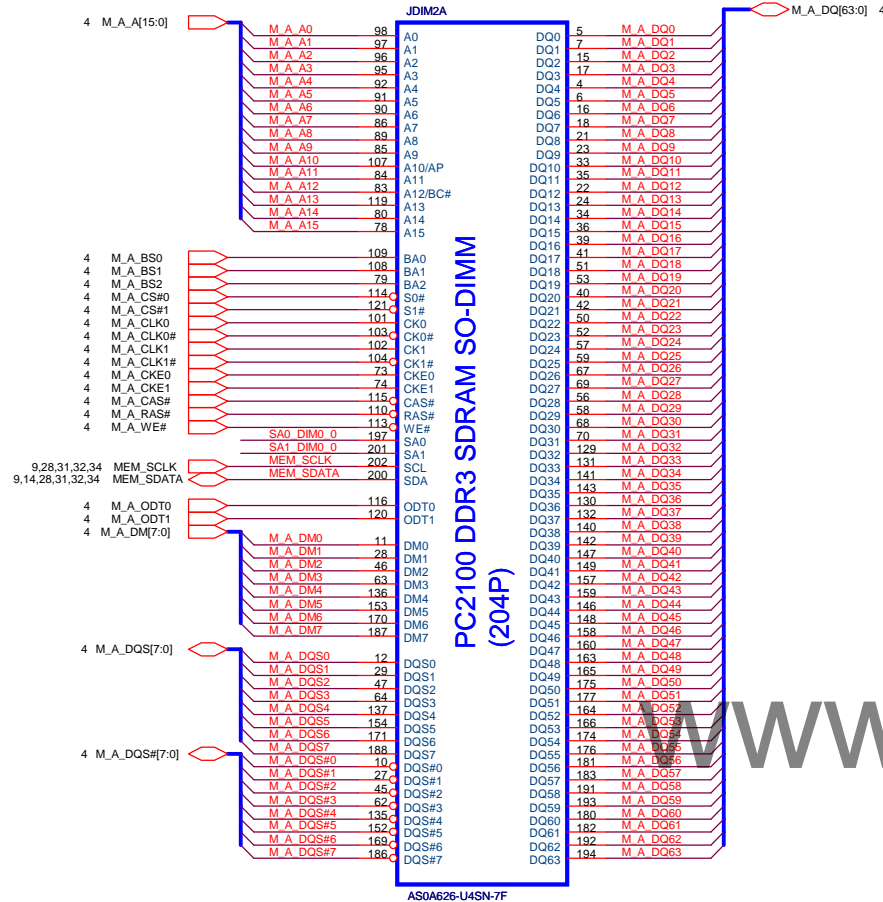
Date: Friday, October 23, 2009 Sheet 11 of 60

# IBEX PEAK-M (GND)



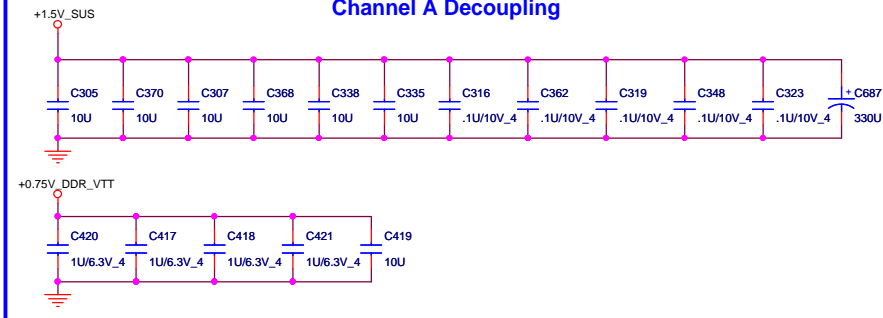
5/13: Change connector from Tyco to Foxconn to avoid shortage

## Channel A



Note:  
If SA1\_DIM0 = 0, SA0\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30  
If SA1\_DIM0 = 0, SA0\_DIM0 = 1  
SO-DIMMA SPD Address is 0xA2  
SO-DIMMA TS Address is 0x32

## Channel A Decoupling



www.aitech1.ru

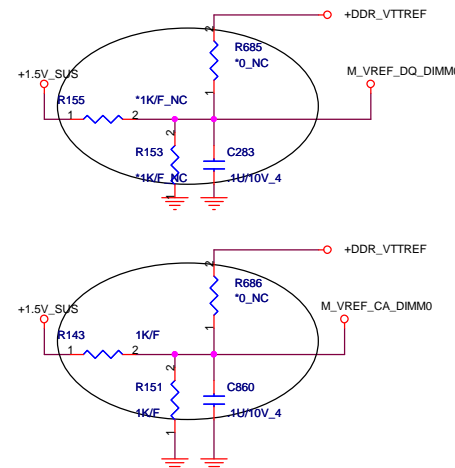
For CH A SO-DIMM VREF\_DQ for M2

Delete according to Intel Design Change

## M1 VREF

5/18: Separate voltage divider for M\_VREF\_DQ\_DIMM0 and M\_VREF\_CA\_DIMM0 to follow Intel CRB design

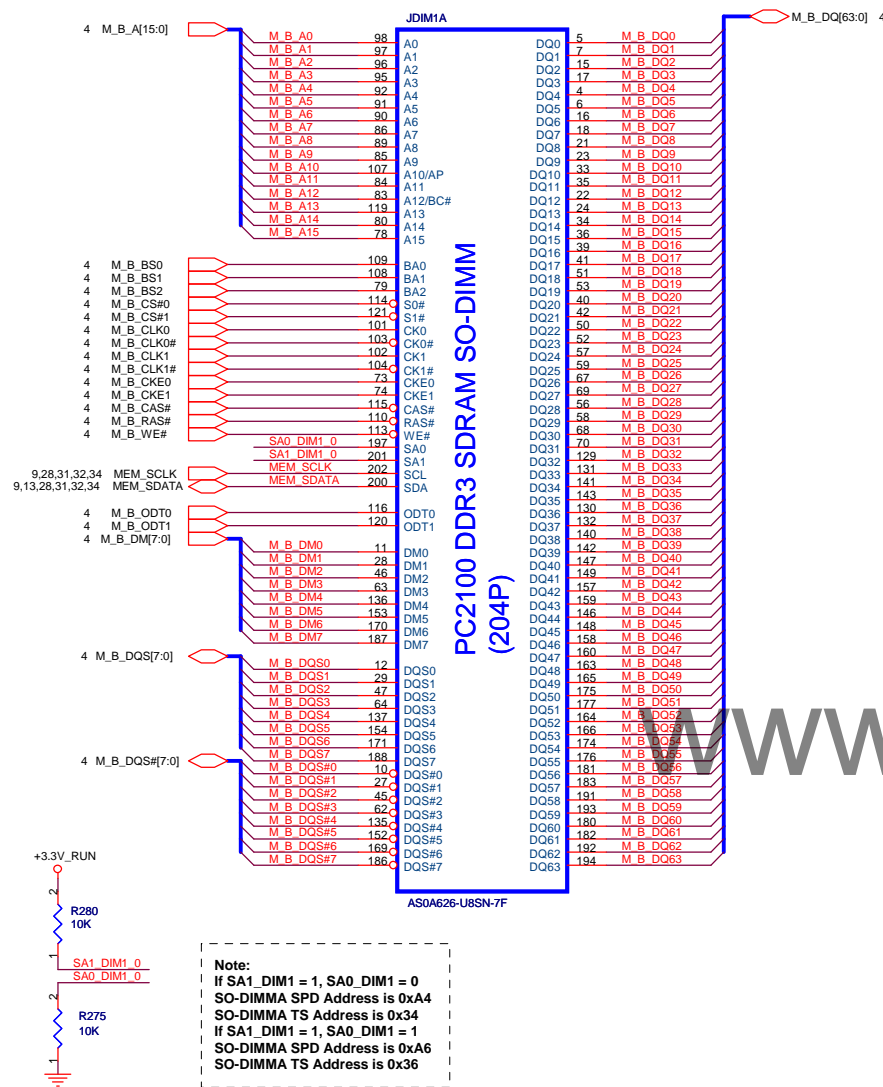
6/02: Change M1 from voltage regulator to voltage divider



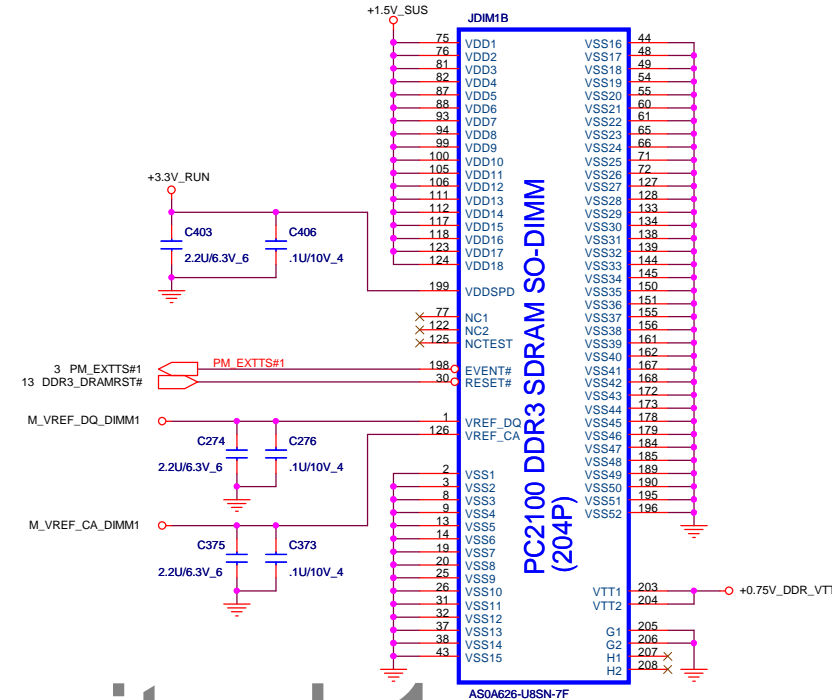
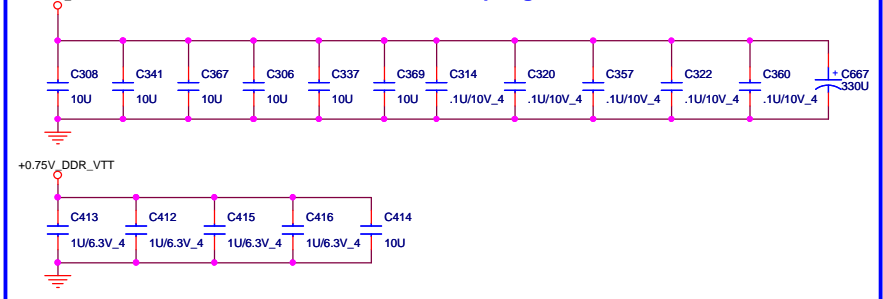
Title			DDR3 DIMM-A
Size	Document Number	Rev	
	RMSC	B1B	
Date:	Friday, October 23, 2009	Sheet	13 of 60

5/13: Change connector from Tyco to Foxconn to avoid shortage

## Channel B



## Channel B Decoupling



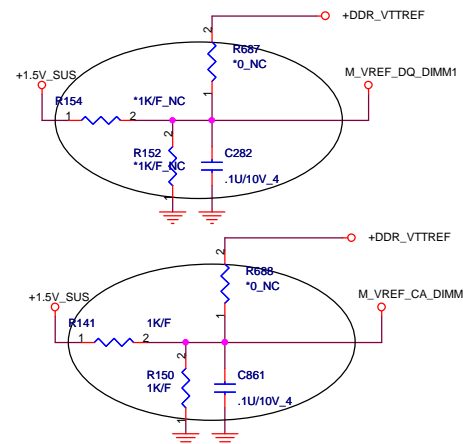
## For CH B SO-DIMM VREF\_DQ for M2

Delete according to Intel Design Change

## M1 VREF

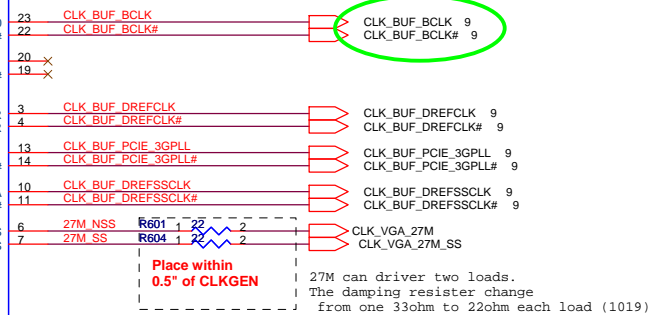
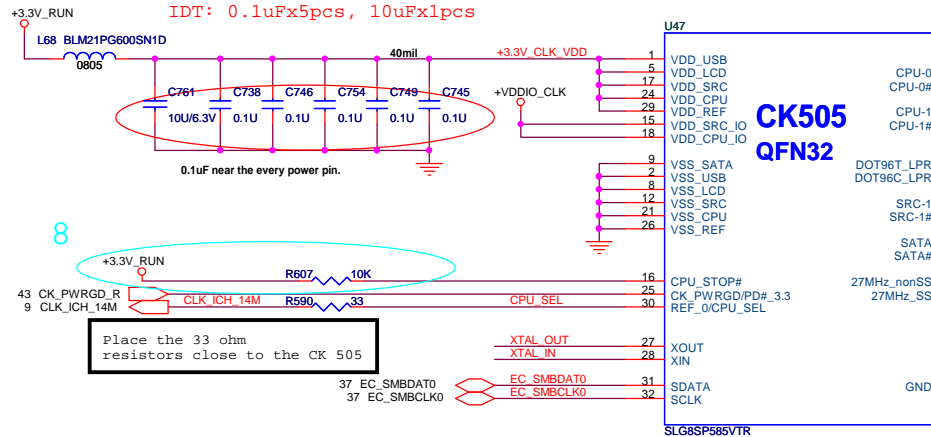
5/18: Separate voltage divider for M\_VREF\_DQ\_DIMM1 and M\_VREF\_CA\_DIMM1 to follow Intel CRB design

6/02: Change M1 from voltage regulator to voltage divider

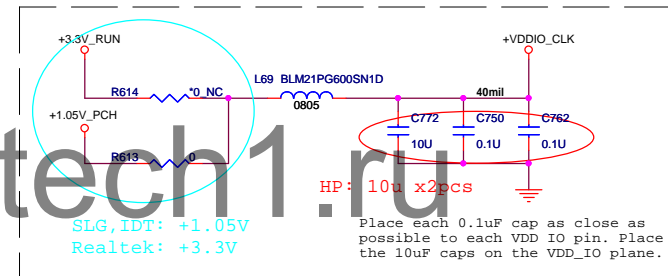


Title			DDR3 DIMM-B
Size	Document Number	Rev	
	RMSC	B1B	
Date:	Friday, October 23, 2009	Sheet	14 of 60

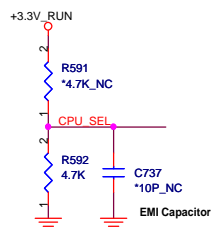
Realtek: 0.1uF x 6pcs, 22uF x 1pcs  
IDT: 0.1uF x 5pcs, 10uF x 1pcs



Realtek: 0.1uF x 3pcs, 22uF x 1pcs  
IDT: 0.1uF x 2pcs, 10uF x 1pcs



+VDDIO\_CLK:  
SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V.  
Realtek date sheet (V1.2) P11: Min 1.05V, Max 3.3V.  
IDT date sheet (V0.7) P10: Min 0.9975V, Max 3.465V.

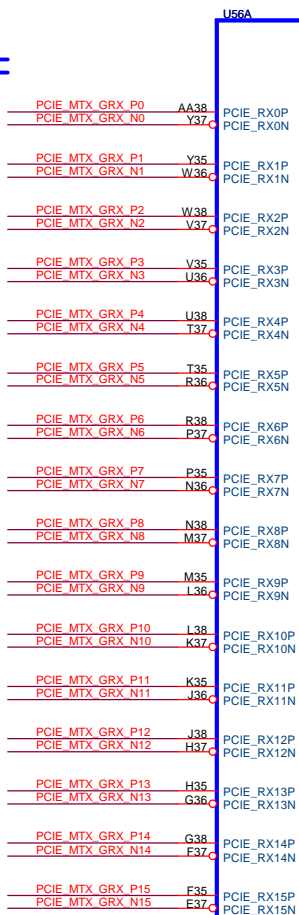


PIN	30	CPU_0	CPU_1
0 (default)		133MHz	133MHz
1 (0.7V-1.5V)		100MHz	100MHz

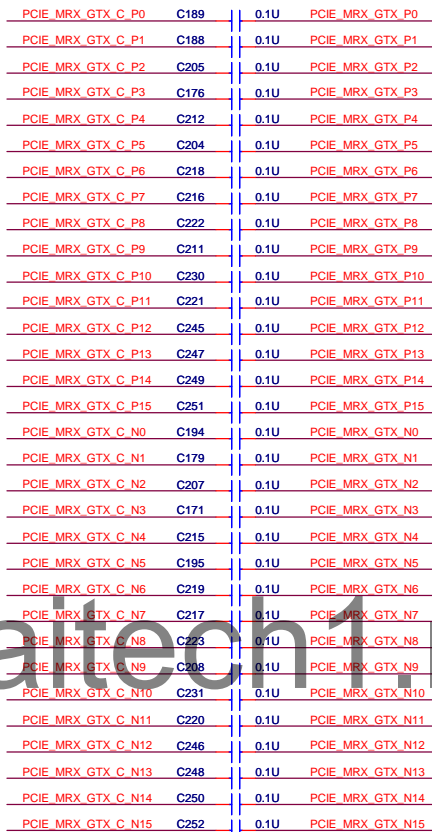
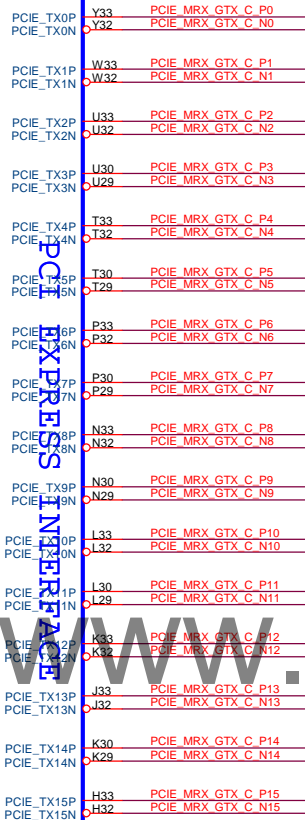
CPU\_SEL:  
SLG date sheet (V0.2) P15:  
High Voltage: Min 0.7V, Max 1.5V.  
Low Voltage: Min Vss-0.3V, Max 0.35V.  
Realtek date sheet (V1.2) P11:  
High Voltage: Min 0.7V, Max 1.5V.  
Low Voltage: Min Vss-0.3V, Max 0.35V.  
IDT date sheet (V0.7) P10:  
High Voltage: Min 0.7V, Max 1.5V.  
Low Voltage: Min Vss-0.3V, Max 0.35V.



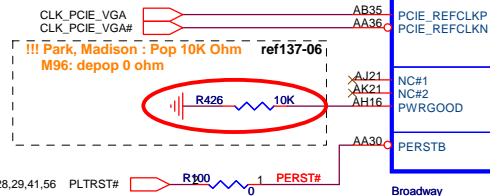
PCIE\_MTX\_GRX\_P[0..15]  
PCIE\_MTX\_GRX\_N[0..15]



PCIE EXPRESS INTERFACE



PCIE\_MRX\_GTX\_P[0..15] 3  
PCIE\_MRX\_GTX\_N[0..15] 3

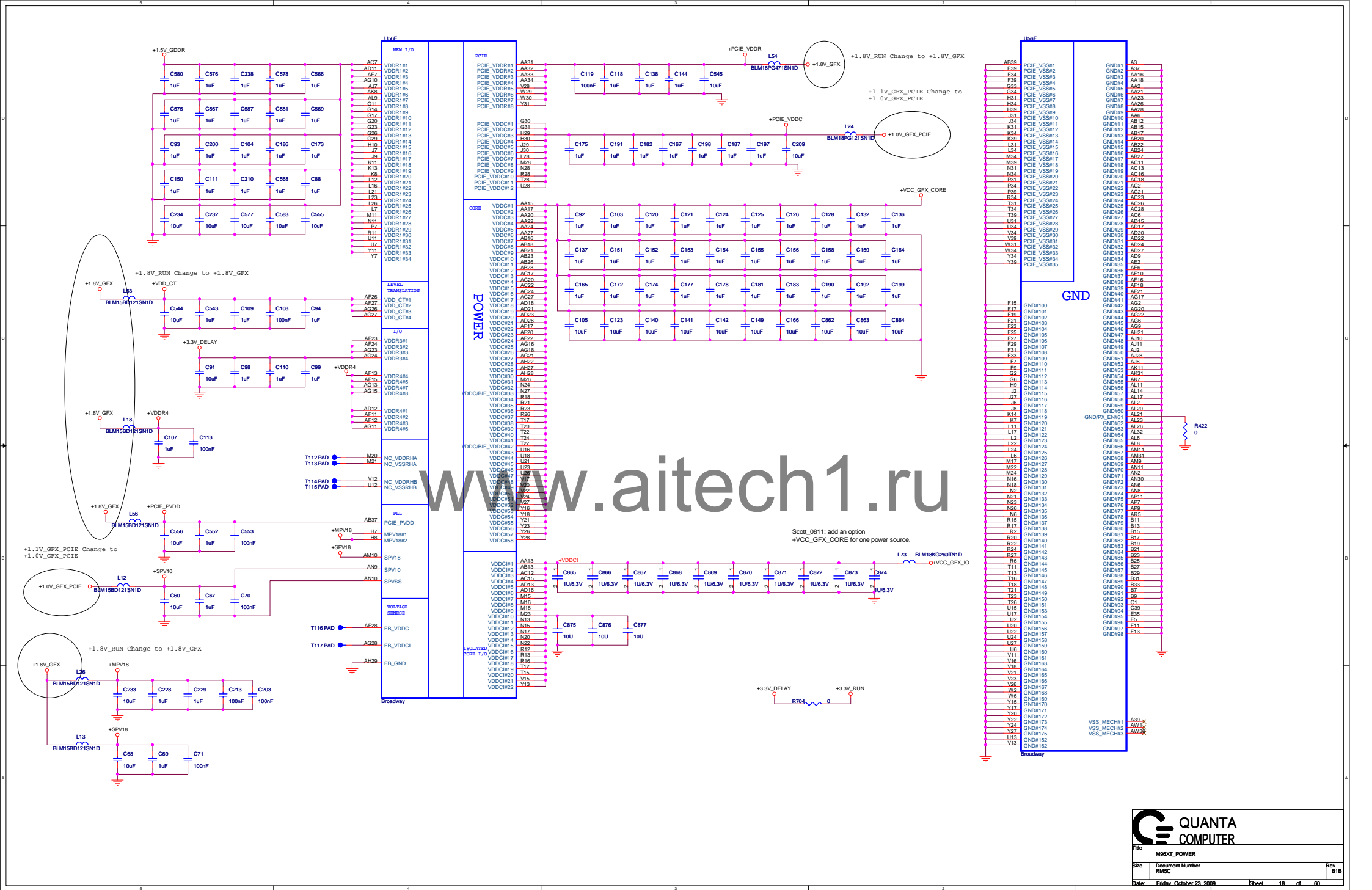


3,26,28,29,41,56 PLTRST# R100 1 PERST#

PWRGOOD should be accessible for test purposes and must be connected to ground for normal operation.







!!!  
For M96/92, DPx\_VDD10 = 1.1V  
For M97 DPx\_VDD10 = 1.0V

ref137-06

1007 for change list

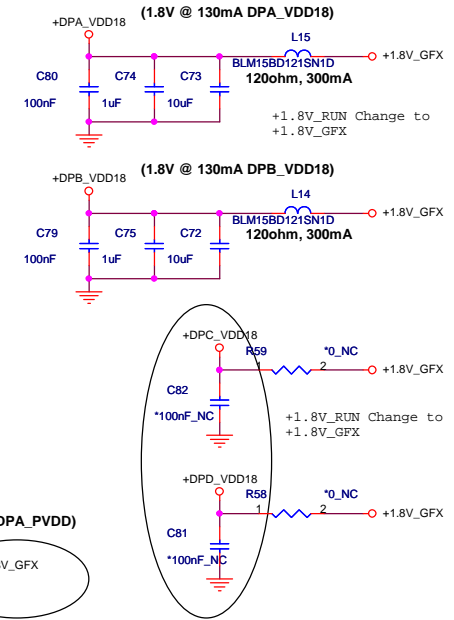
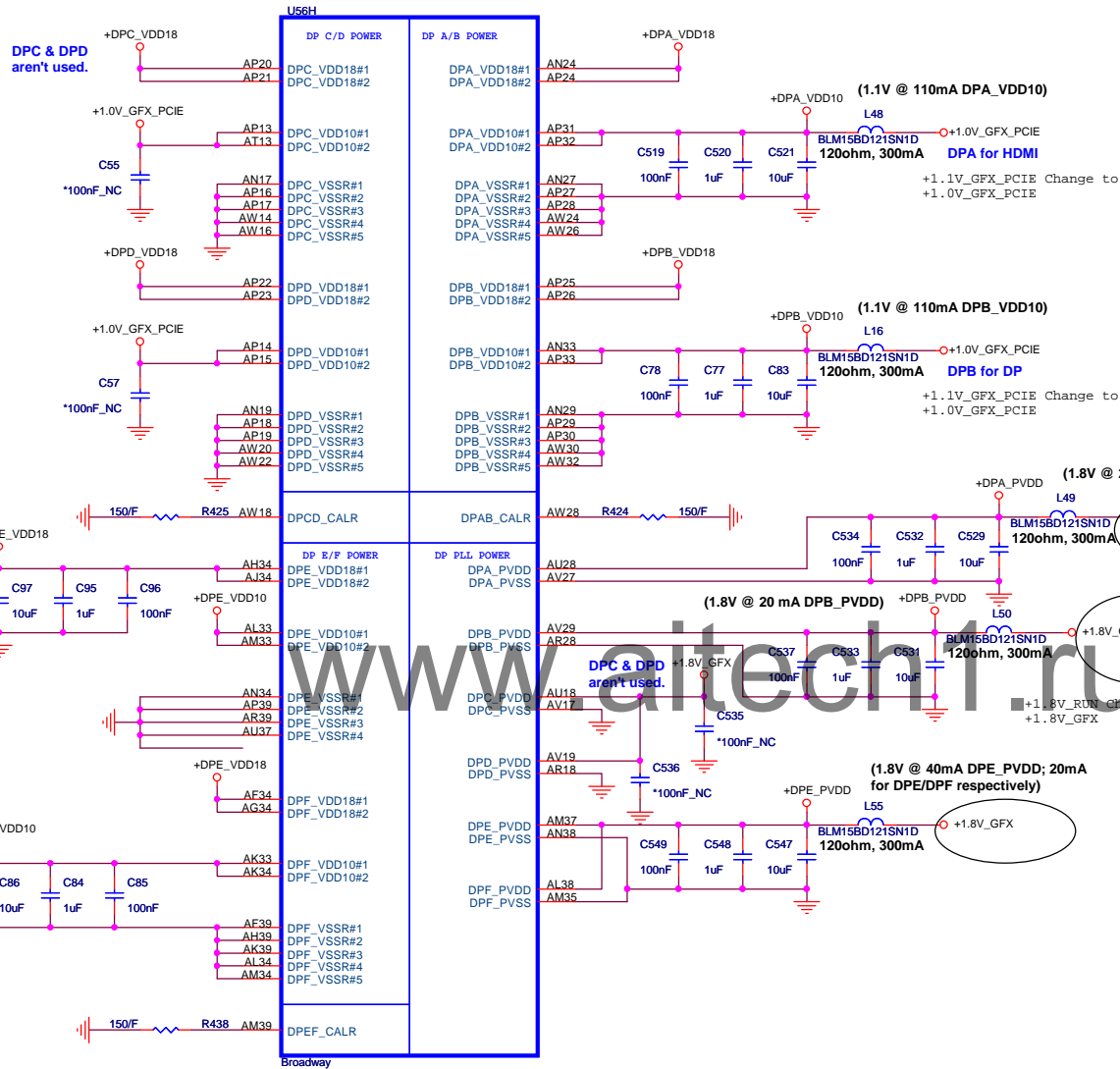
(1.8V @ 400mA DPE\_VDD18;  
200mA for DPE/DPF respectively)

0504: Change L19 for low DCR  
0.1ohm as AMD suggest.

DPE & DPF for LVDS

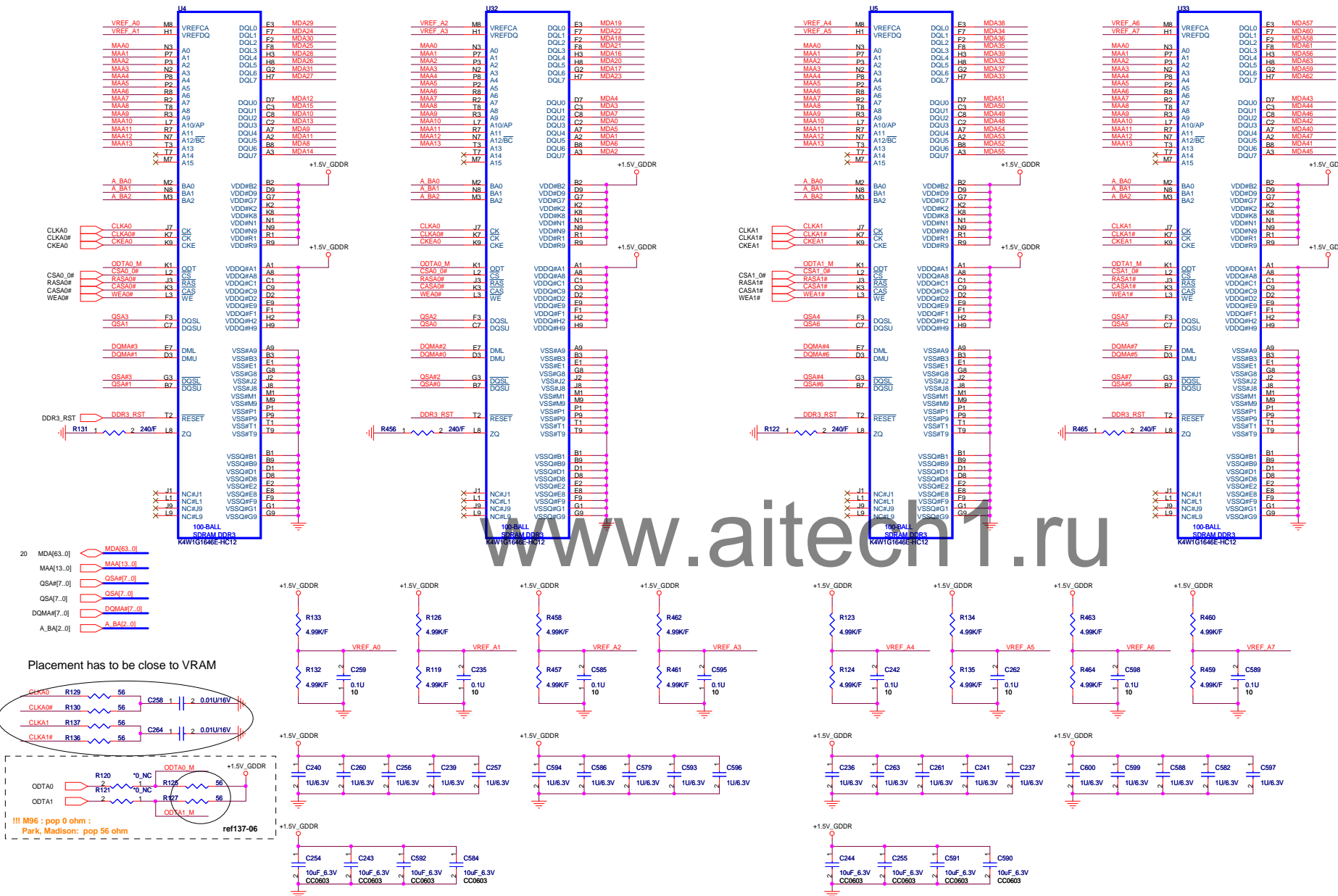
(1.1V @ 200mA DPE\_VDD10;  
100mA for DPE/DPF respectively)

+1.1V\_GFX\_PCIE Change to  
+1.0V\_GFX\_PCIE



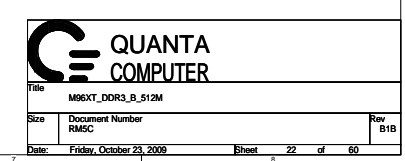


# DDR3 64MX16, CH A : 512MB

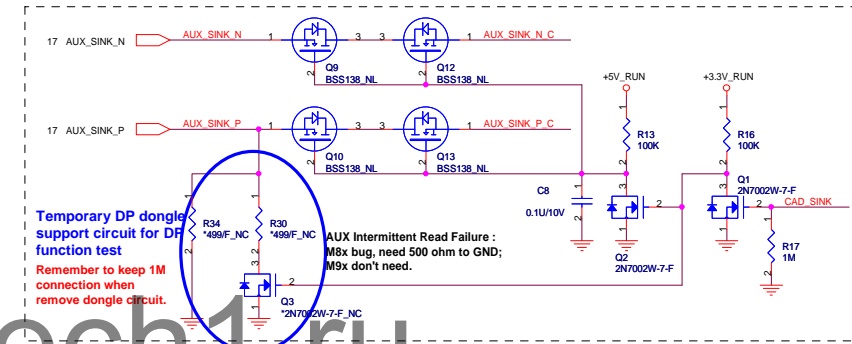
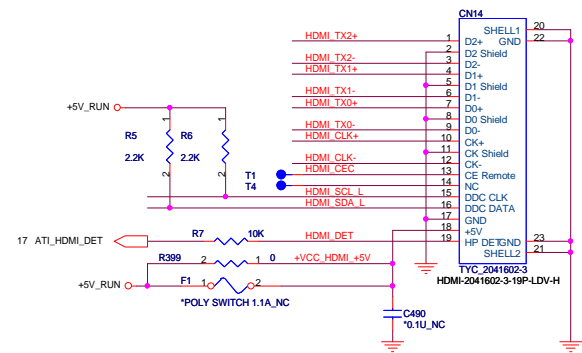


File: M96XT\_DDR3\_A\_512M

Size: Document Number  
RMSD  
Date: Friday, October 23, 2009 Sheet: 21 of 60







Delete EMI ESD IC for EMI asked HDMI signals link to CONN directly.

**Temporary DP dongle support circuit for DP function test**

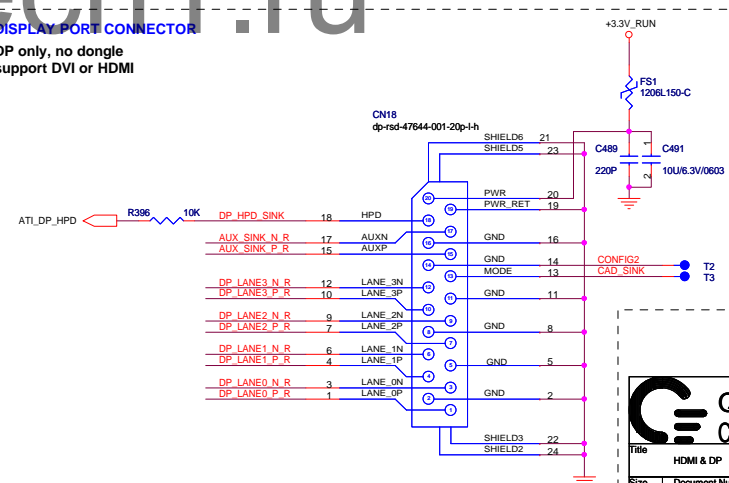
**Remember to keep 1M connection when remove dongle circuit.**

**AUX Intermittent Read Failure :**  
M8x bug, need 500 ohm to GND;  
M9x don't need.

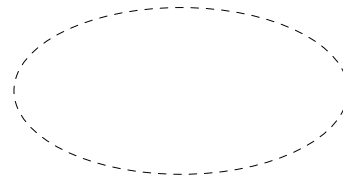



The diagram shows a circuit for testing DP (DisplayPort) functionality. It features a DP connector with pins 1 through 30. A 1M resistor (R34) is connected between pins 1 and 2. A 500 ohm resistor (R30) is connected between pin 1 and GND. A DP dongle (Q3) is connected between pins 1 and 2. The circuit is labeled 'Temporary DP dongle support circuit for DP function test' and 'Remember to keep 1M connection when remove dongle circuit.'.

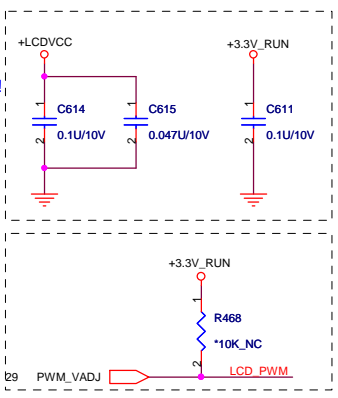
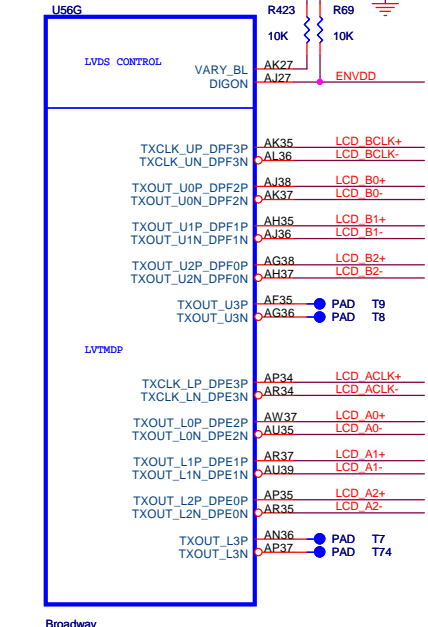
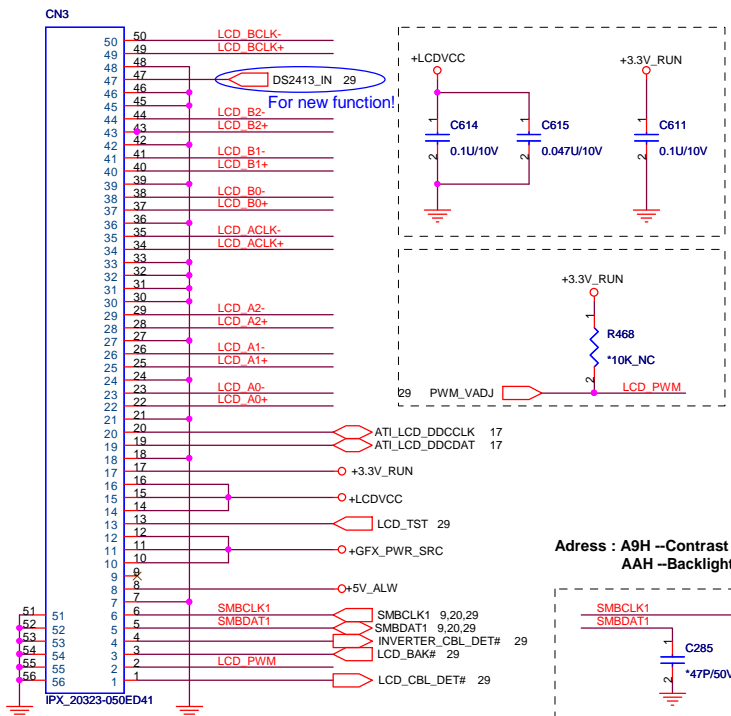
**DISPLAY PORT CONNECTOR**  
DP only, no dongle  
support DVI or HDMI



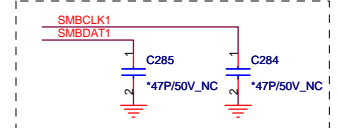
Scott\_0703:Delete ESD Clamp U23,U24,U25 as EMI suggestion.



 <b>QUANTA COMPUTER</b>			
Title <b>HDMI &amp; DP</b>			
Size	Document Number <b>RM5C</b>		Rev <b>B1B</b>
Date:	<b>Friday, October 23, 2009</b>	Sheet <b>23</b> of <b>60</b>	

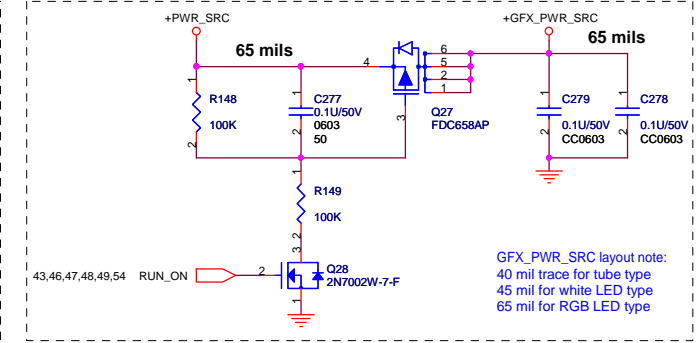
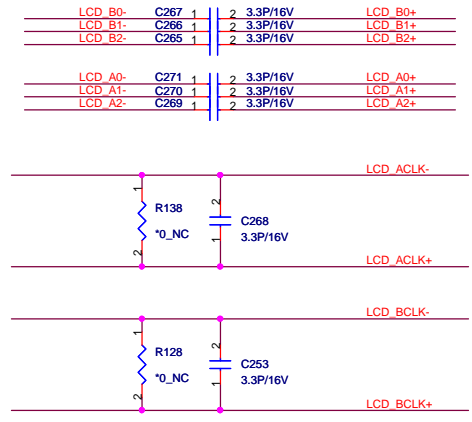


Address : A9H --Contrast  
AAH --Backlight

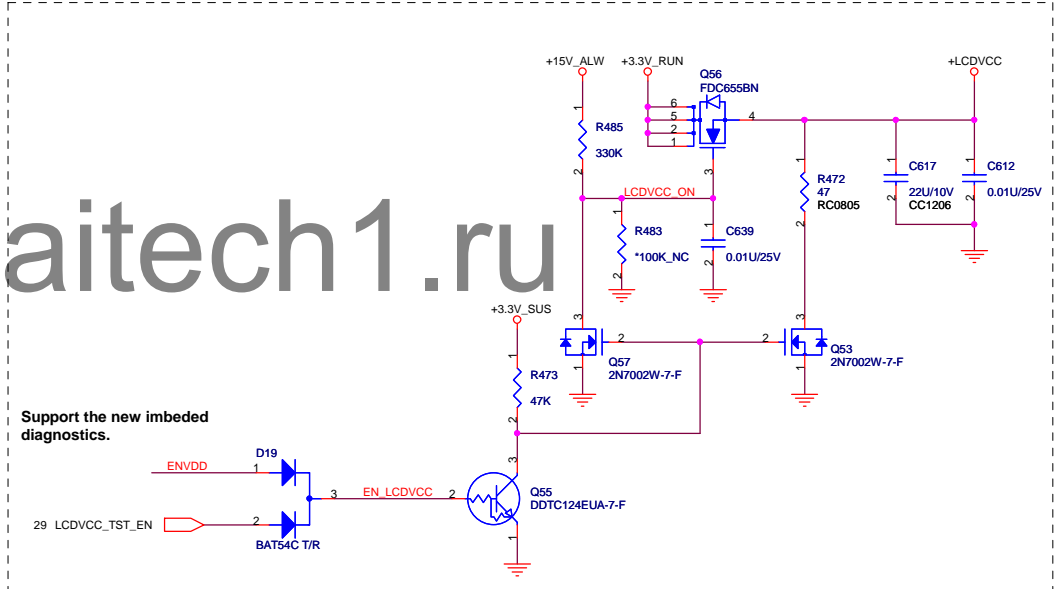


Scott\_0812: Delete DPST function as non-used.

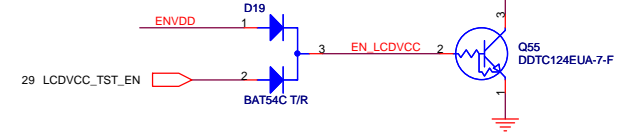
### Shunt capacitors on LVDS for improving WWAN.

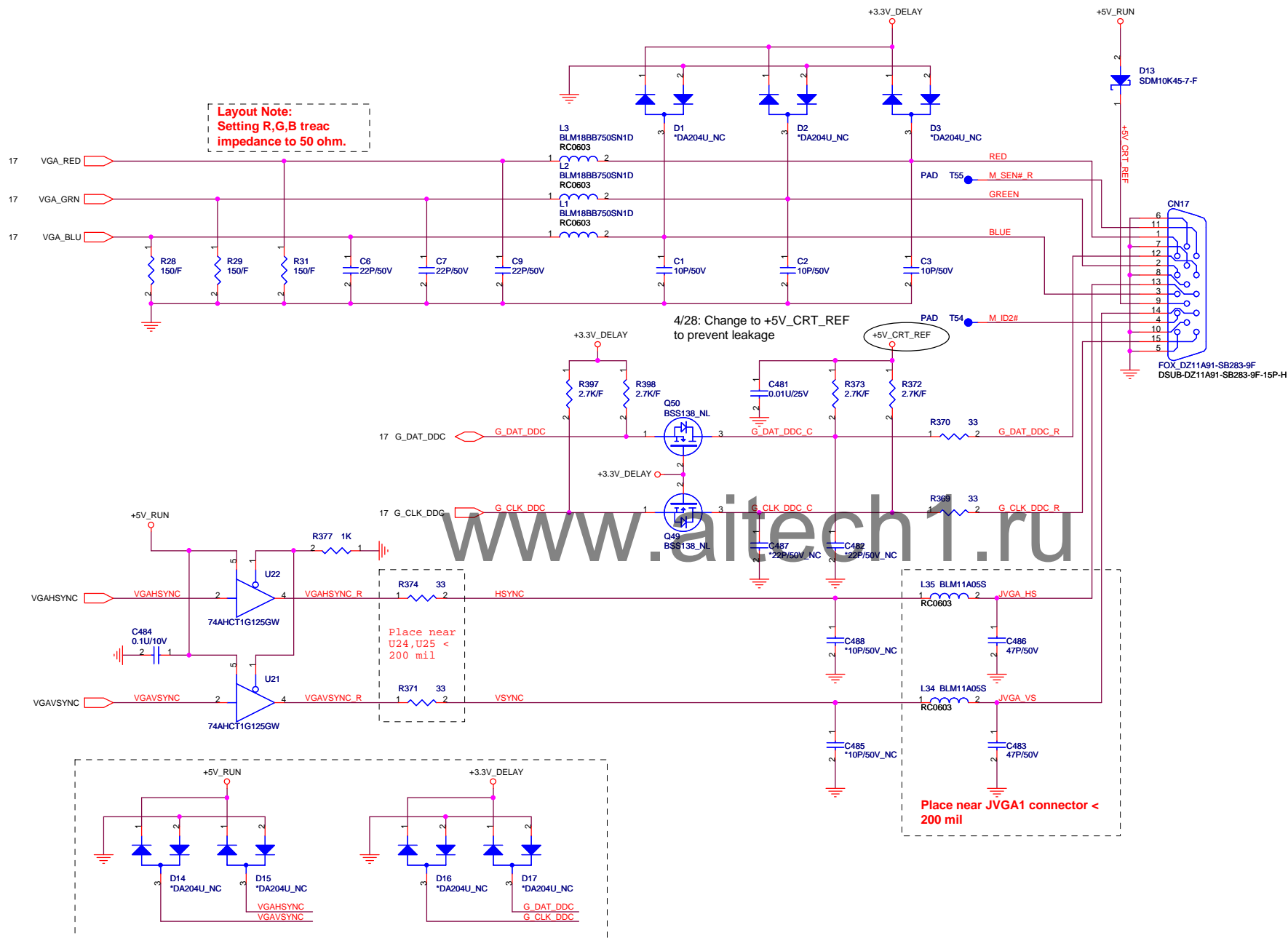


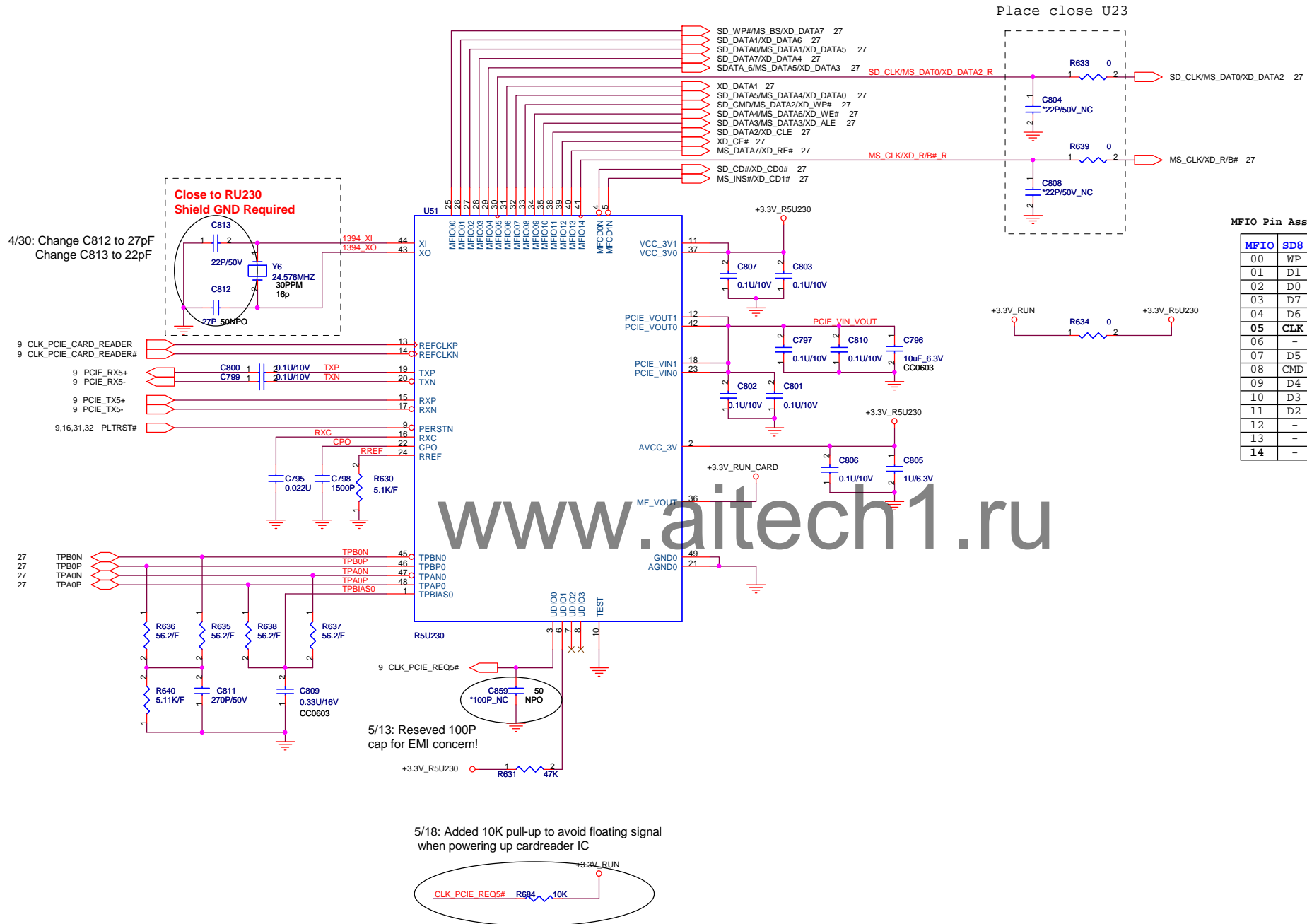
GFX\_PWR\_SRC layout note:  
40 mil trace for tube type  
45 mil for white LED type  
65 mil for RGB LED type



Support the new imbedded diagnostics.







MFIO Pin Assignment Table

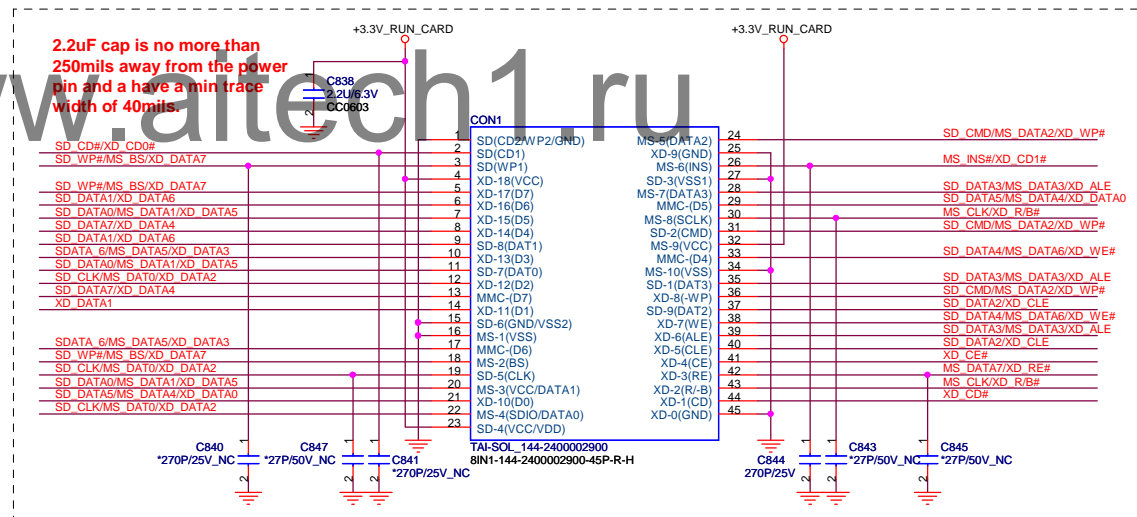
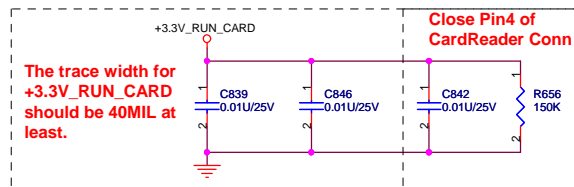
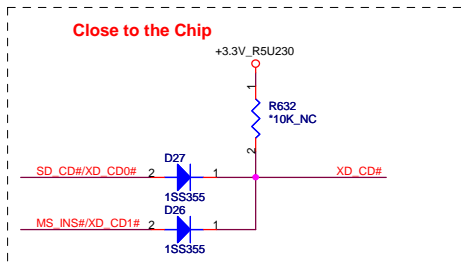
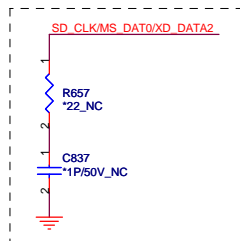
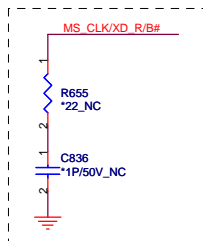
MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	-	D6
02	D0	D1	D5
03	D7	-	D4
04	D6	D5	D3
05	CLK	D0	D2
06	-	-	D1
07	D5	D4	D0
08	CMD	D2	WP#
09	D4	D6	WE#
10	D3	D3	ALE
11	D2	-	CLE
12	-	-	CE#
13	-	D7	RE#
14	-	CLK	R/B#



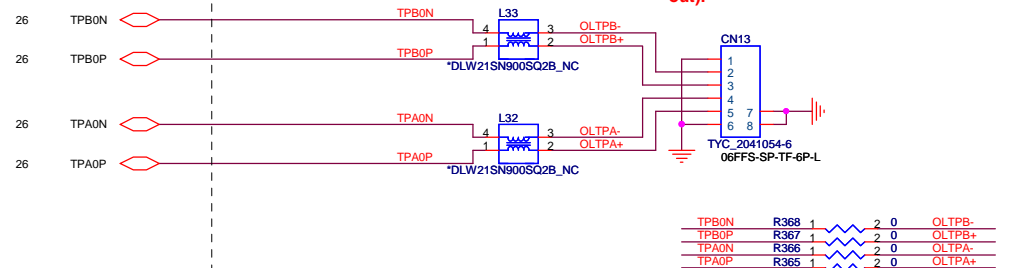
Title CardReader (5C833)		
Size Document Number RMSC	Rev B1B	
Date: Friday, October 23, 2009	Sheet 26	of 60

26 SD\_WP#/MS\_BS/XD\_DATA7  
 26 SD\_DATA1/XD\_DATA6  
 26 SD\_DATA0/MS\_DATA1/XD\_DATA5  
 26 SD\_DATA7/XD\_DATA4  
 26 SDATA\_6/MS\_DATA5/XD\_DATA3  
 26 SD\_CLK/MS\_DATA0/XD\_DATA2  
 26 XD\_DATA1  
 26 SD\_DATA5/MS\_DATA4/XD\_DATA0  
 26 SD\_CMD/MS\_DATA2/XD\_WP#  
 26 SD\_DATA4/MS\_DATA6/XD\_WE#  
 26 SD\_DATA3/MS\_DATA3/XD\_ALE  
 26 SD\_DATA2/XD\_CLE  
 26 XD\_CE#  
 26 MS\_DATA7/XD\_RE#  
 26 MS\_CLK/XD\_R/B#  
 26 SD\_CD#/XD\_CD0#  
 26 MS\_INS#/XD\_CD1#

SD\_WP#/MS\_BS/XD\_DATA7  
 SD\_DATA1/XD\_DATA6  
 SD\_DATA0/MS\_DATA1/XD\_DATA5  
 SD\_DATA7/XD\_DATA4  
 SDATA\_6/MS\_DATA5/XD\_DATA3  
 SD\_CLK/MS\_DATA0/XD\_DATA2  
 XD\_DATA1  
 SD\_DATA5/MS\_DATA4/XD\_DATA0  
 SD\_CMD/MS\_DATA2/XD\_WP#  
 SD\_DATA4/MS\_DATA6/XD\_WE#  
 SD\_DATA3/MS\_DATA3/XD\_ALE  
 SD\_DATA2/XD\_CLE  
 XD\_CE#  
 MS\_DATA7/XD\_RE#  
 MS\_CLK/XD\_R/B#  
 SD\_CD#/XD\_CD0#  
 MS\_INS#/XD\_CD1#

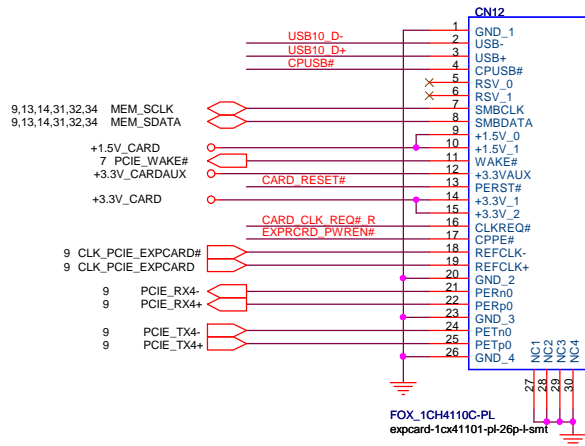


# Reserved EMI Solution



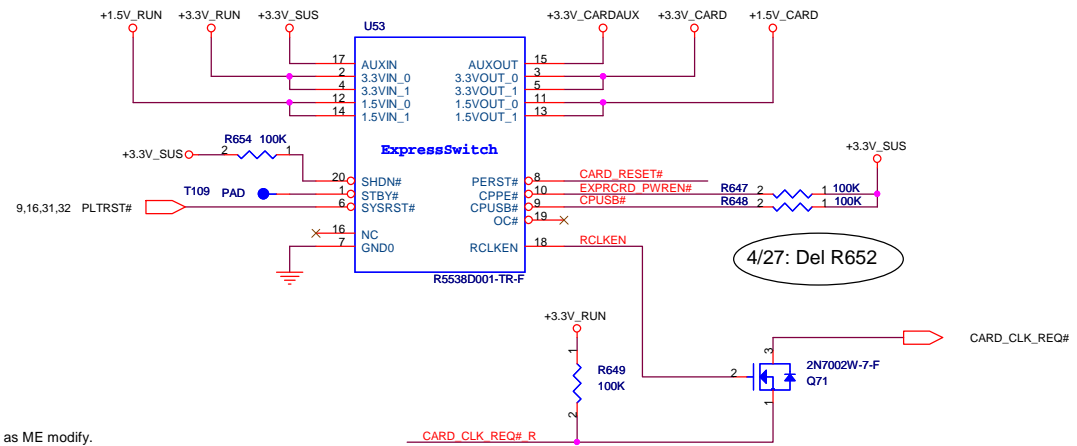
Title		
8 IN 1 & 1394 CONN		
Size	Document Number	Rev
	RMSC	B1B
Date:	Friday, October 23, 2009	Sheet 27 of 60

## Express Card



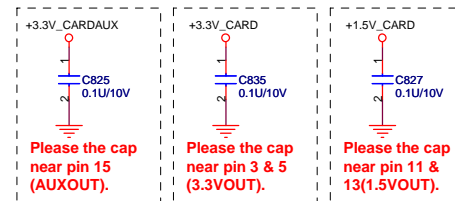
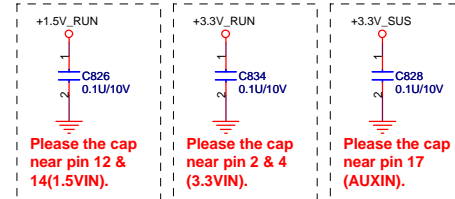
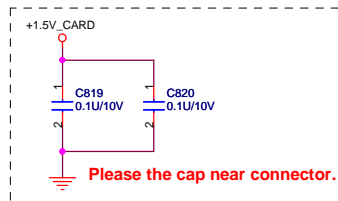
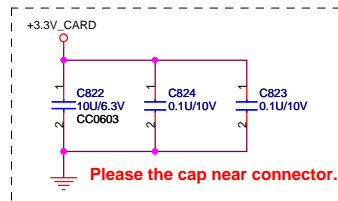
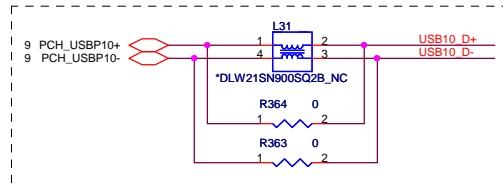
Scott\_0813:Change CN12 F/P to expcard-1cx41101-pl-26p-l-smt as ME modify.

+1.5V\_CARD Max. 650mA, Average 500mA.  
+3V\_CARD Max. 1300mA, Average 1000mA.



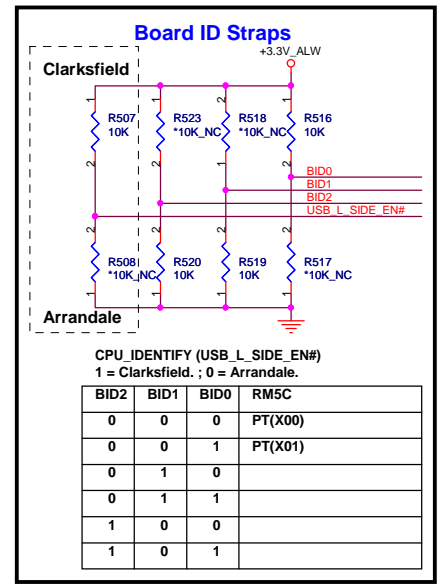
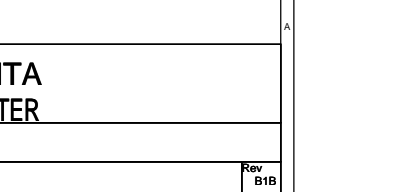
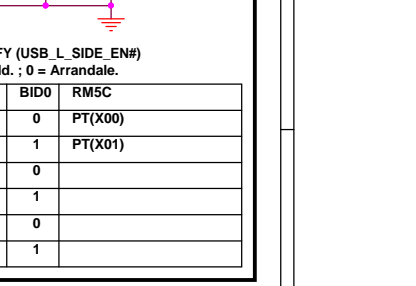
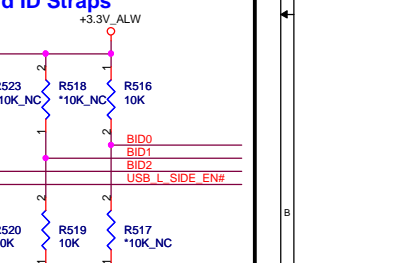
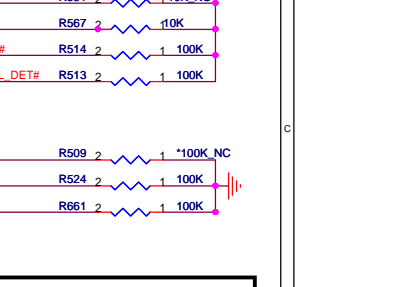
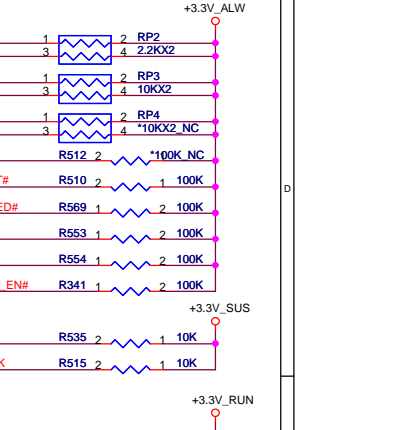
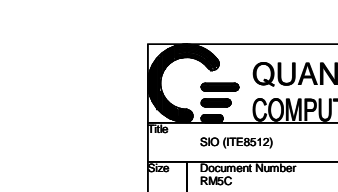
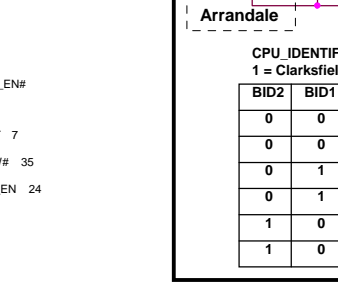
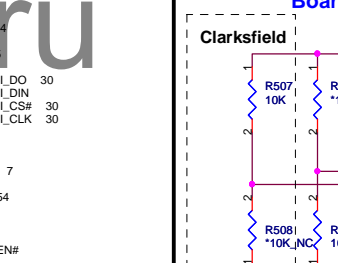
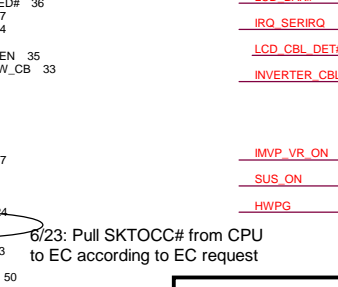
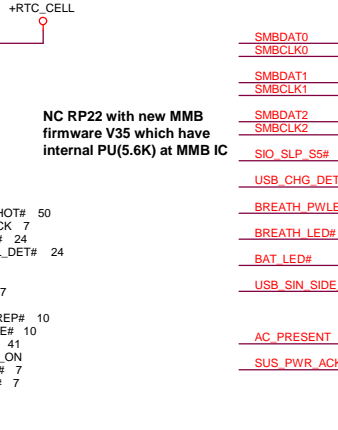
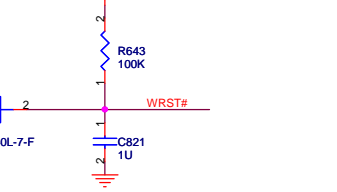
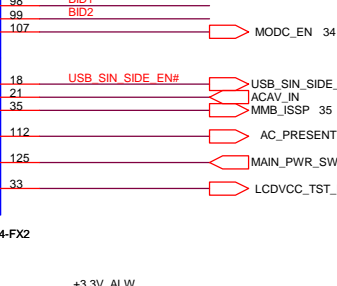
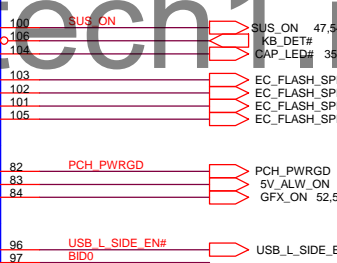
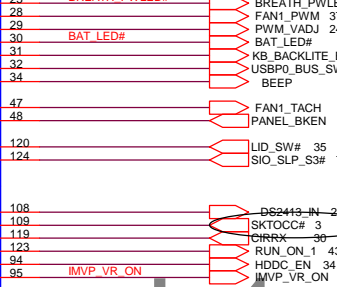
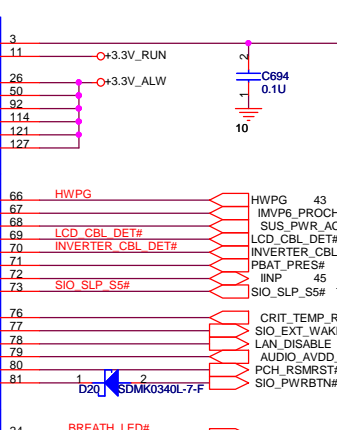
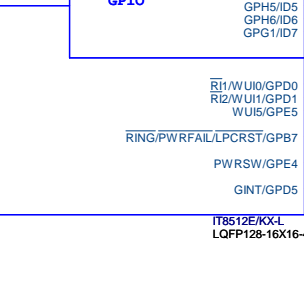
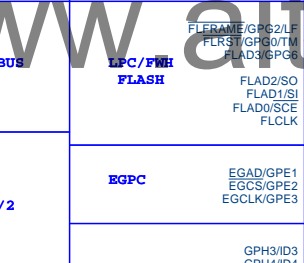
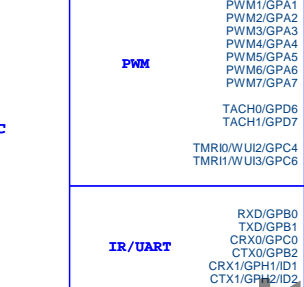
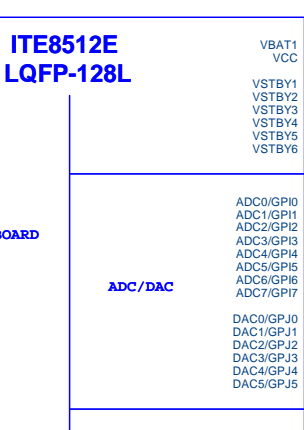
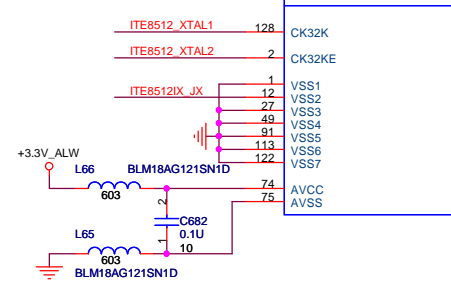
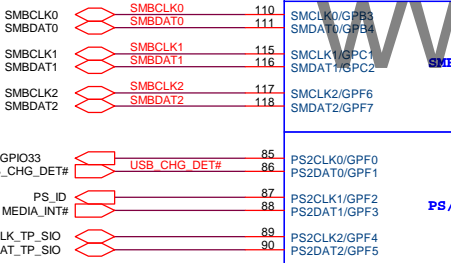
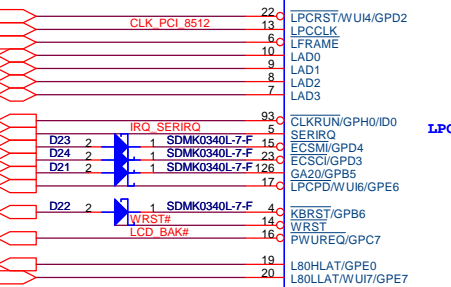
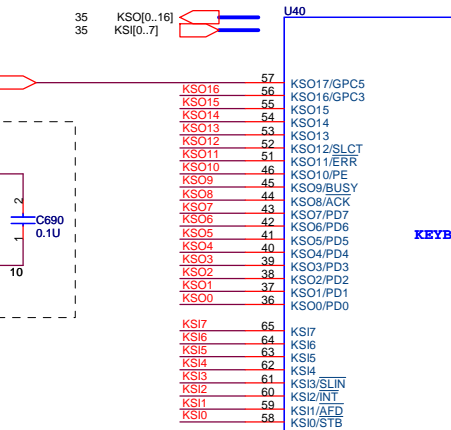
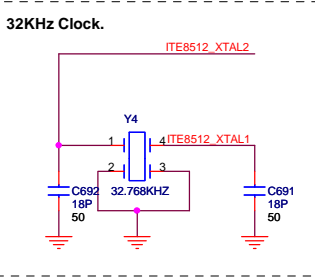
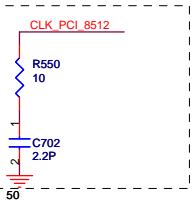
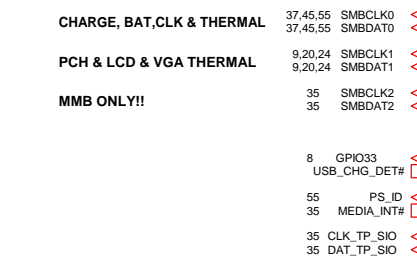
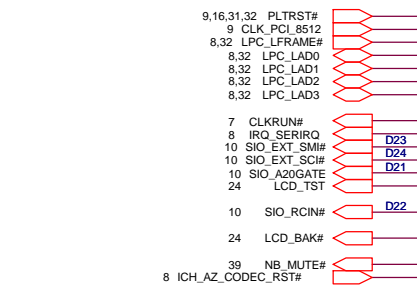
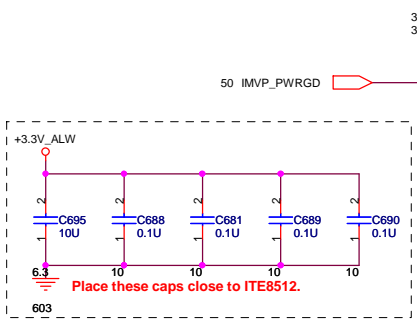
www.aitech1.ru

### PCI-Express TX and RX direct to connector.



Title EXPRESS CARD		
Size	Document Number RMSC	Rev B1B
Date:	Friday, October 23, 2009	Sheet 28 of 60





**QUANTA COMPUTER**

Title: SIO (ITE8512)

Size: Document Number RM5C

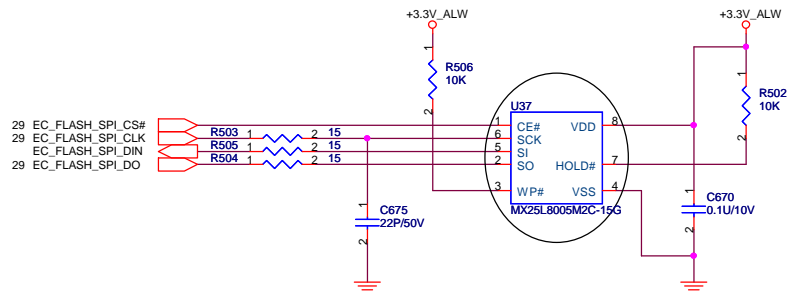
Date: Friday, October 23, 2009

Sheet: 29 of 60

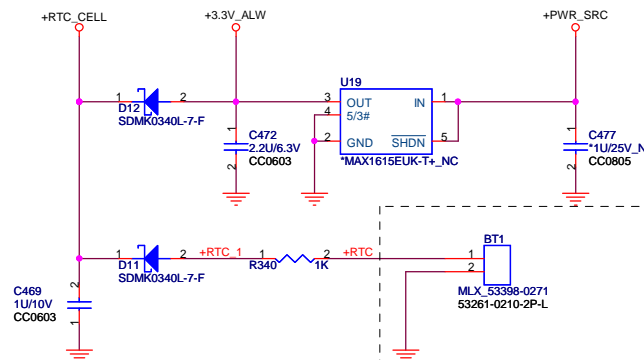
Rev: B1B

# EC SPI ROM, 8Mbit (1M Byte)

5/12: Change U37 from 2MB to 1MB according to BIOS request!

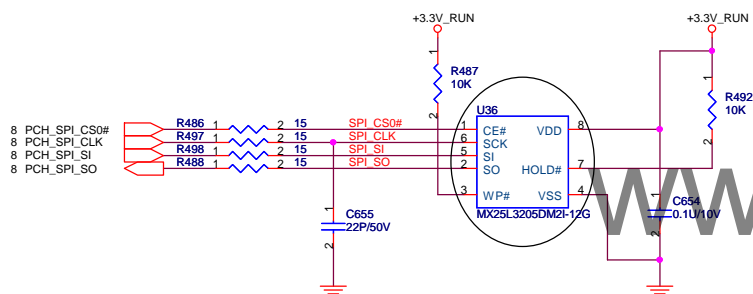


# RTC BATTERY

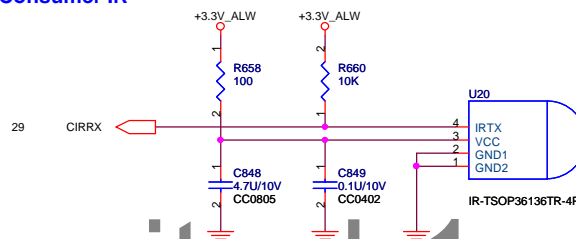


# PCH SPI ROM, (4M Byte)

5/12: Change U36 from 2MB to 4MB according to BIOS request!

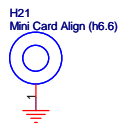


# Consumer IR



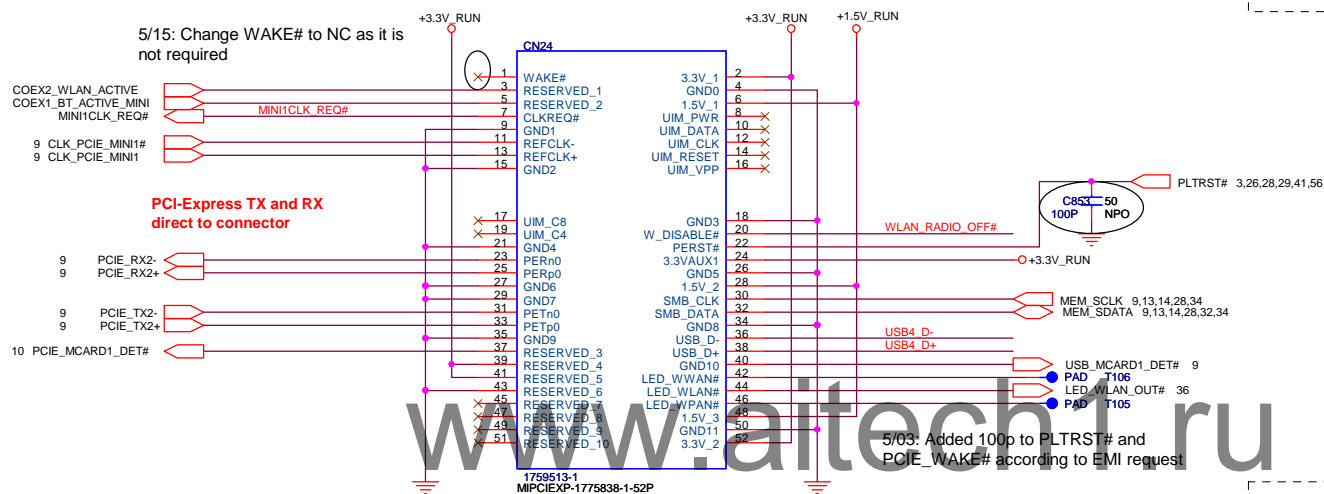
Title			FLASH/ RTC/ CIR
Size	Document Number	Rev	
	RM5C	B1B	
Date:	Friday, October 23, 2009	Sheet	30 of 60

# Mini Card Nut



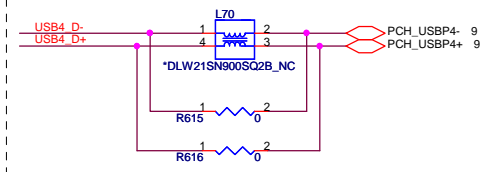
## MiniCard WLAN Connector

5/15: Change WAKE# to NC as it is not required



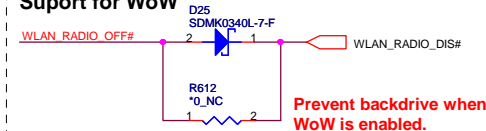
PCI-Express TX and RX direct to connector

### Reserved PAD for EMI

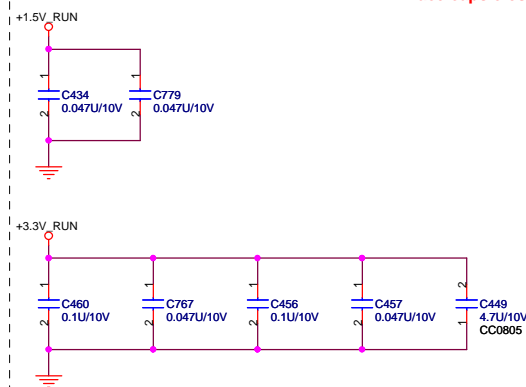


5/03: Added 100p to PLTRST# and PCIE\_WAKE# according to EMI request

### Support for WoW



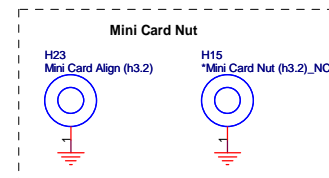
Place caps close to connector.



Title MINI-CARD (WLAN)		
Size	Document Number RM5C	Rev B1B
Date:	Friday, October 23, 2009	Sheet 31 of 60

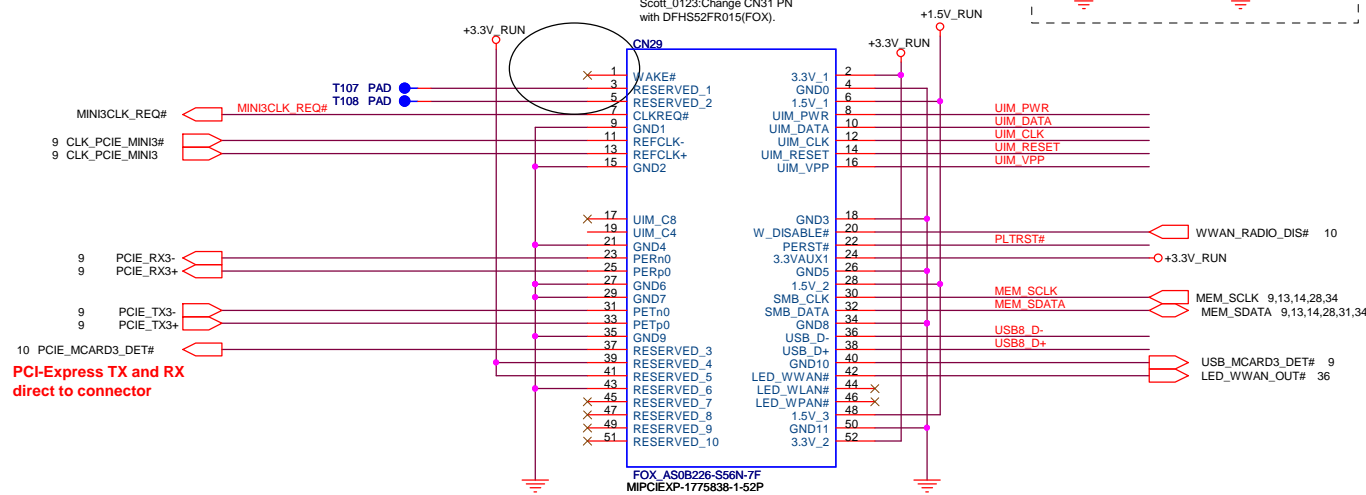
5/15: Change WAKE# to NC as it is not required

## MiniCard WWAN Connector

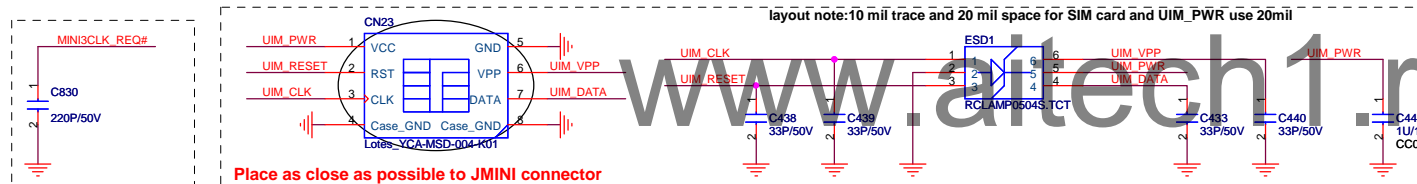


**Layout Note:**

**Layout Note:** R240 and R244 close to choke as possible to minimize stubs.



### 5/13: Change SIM card connector to Lotes



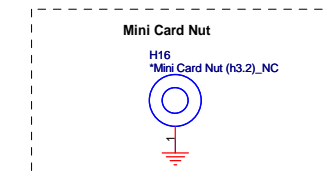
**Place as close as possible to JMINI connector**

**Layout Note:**

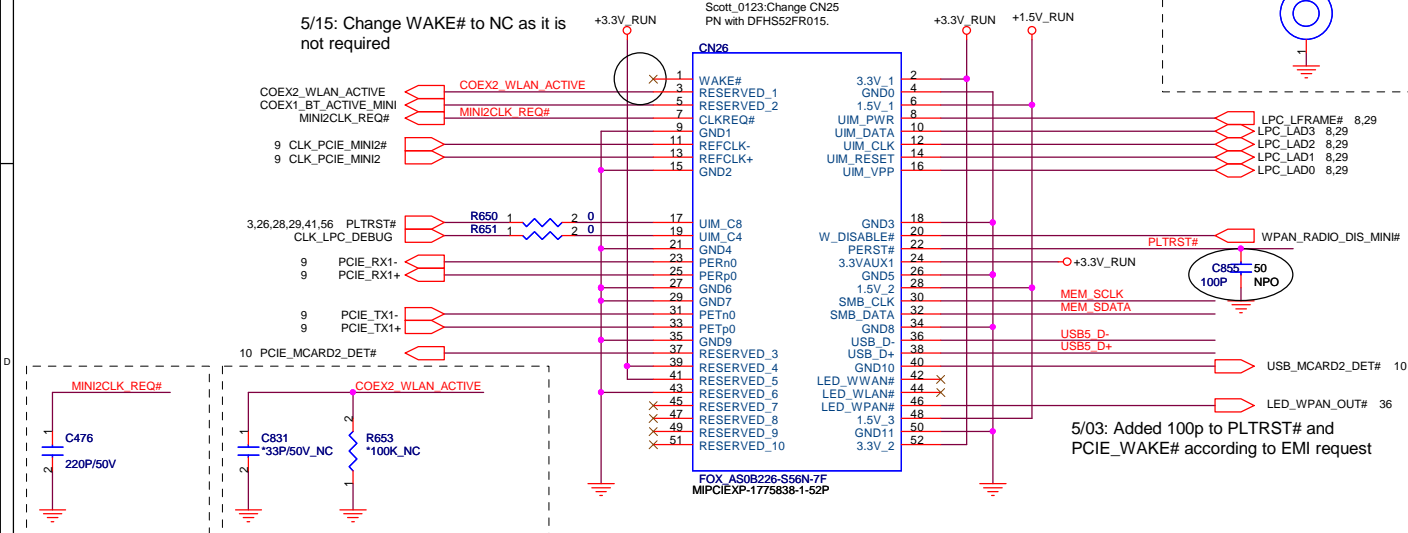
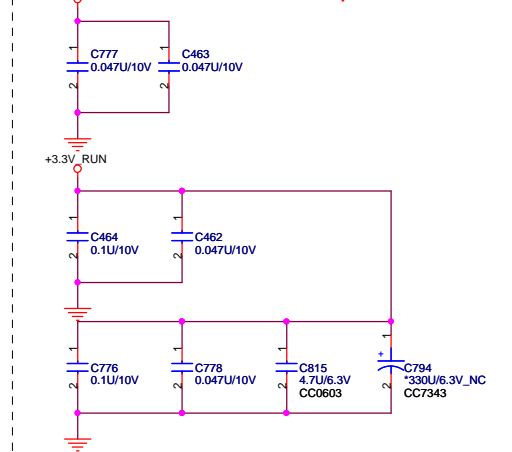
**Layout Note:** R240 and R244 close to choke as possible to minimize stubs.

### MiniCard Robson, BT. UWB Connector

Scott\_0123:Change CN2  
PN with DFHS52FR015.



+1.5V RUN **Place caps close to connector.**

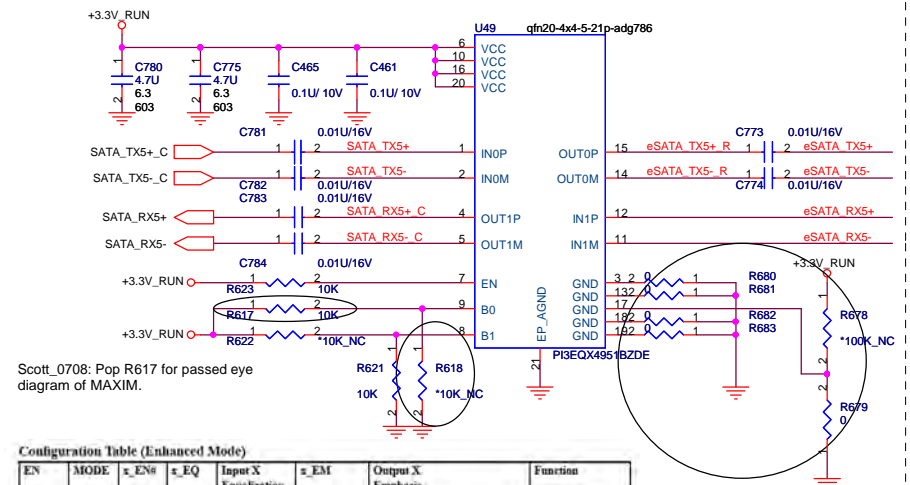


5/03: Added 100p to PLTRST# and  
PCIE\_WAKE# according to EMI request



Title			
MINI-CARD (WPAN,WWAN)			
Size	Document Number	Rev	B1B
	RMSC		
Date:	Friday, October 23, 2009	Sheet	32 of 60

eSATA Re-driver IC

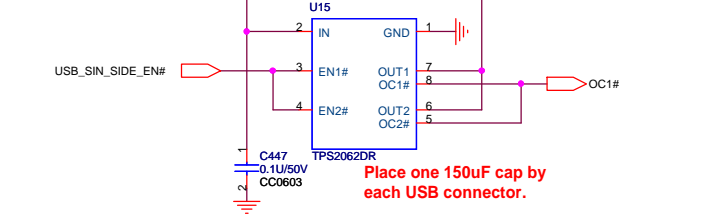


Configuration Table (Enhanced Mode)

EN	MODE	$\pm$ EN#	$\pm$ EQ	Input X Equalization	$\pm$ EM	Output X Emphasis	Function
0	X	X	X	n/a	X	n/a	Chip Power Down:
1	1	1	X	n/a	X	n/a	Chip enabled, Channel x disabled
1	1	0	0	2.5dB	1.1K to 15K resistor	Resistor Controlled, 6dB to 0dB (0)	Chip and channel enabled, low input equalization
1	1	0	1	6.5dB	1.1K to 15K resistor	Resistor Controlled, 6dB to 0dB (0)	Chip and channel enabled, high input equalization

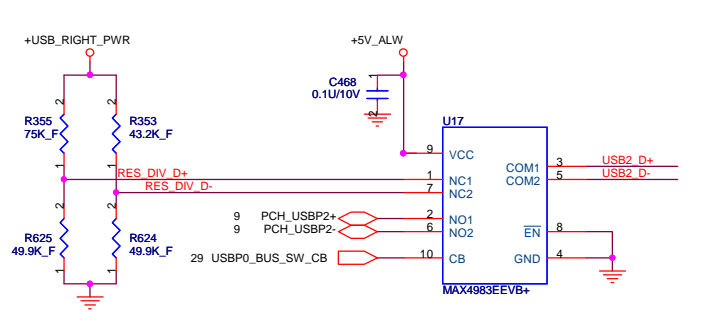
5/11: Reserved 0 ohms for Pericom enhanced mode select,  
5/12: Change IC to Pericom as Maxim failed EA test  
6/23: NC according to Pericom recommendation!

USB POWER SW  
Each channel is 1A

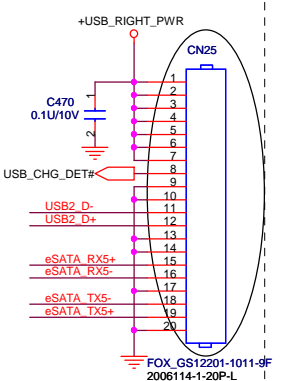


Place one 150uF cap by each USB connector.

USB Power Share

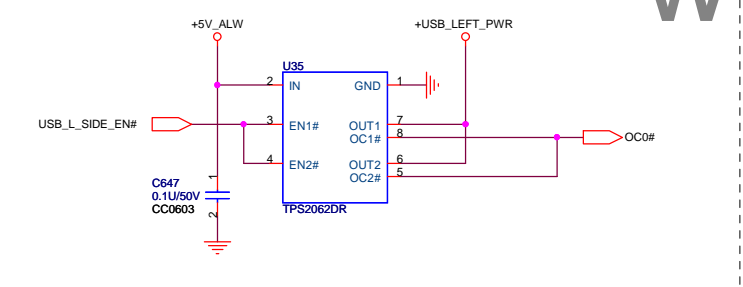


eSATA CONN

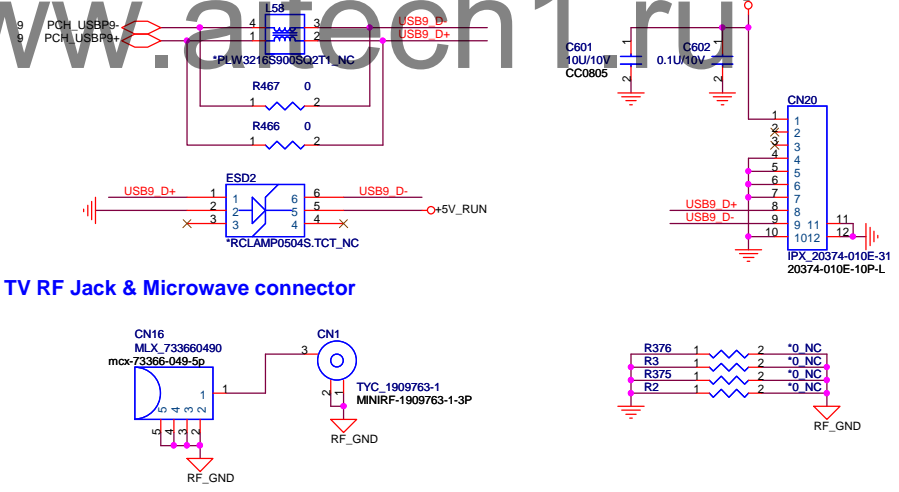


5/13: Change Connector to Foxconn to avoid material shortage for Tyco

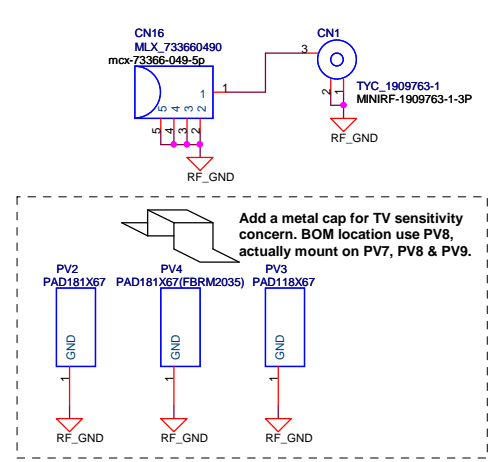
USB POWER SW  
Each channel is 1A



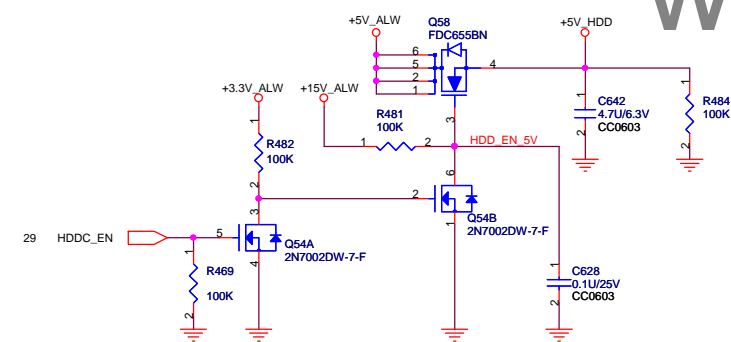
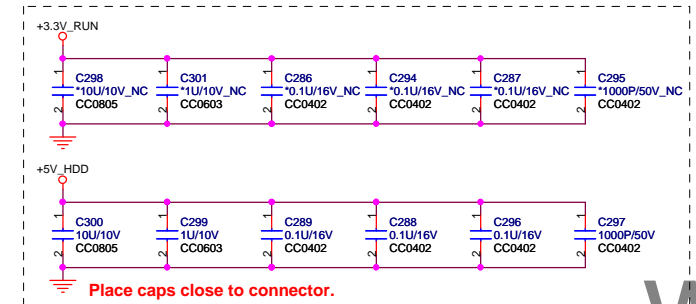
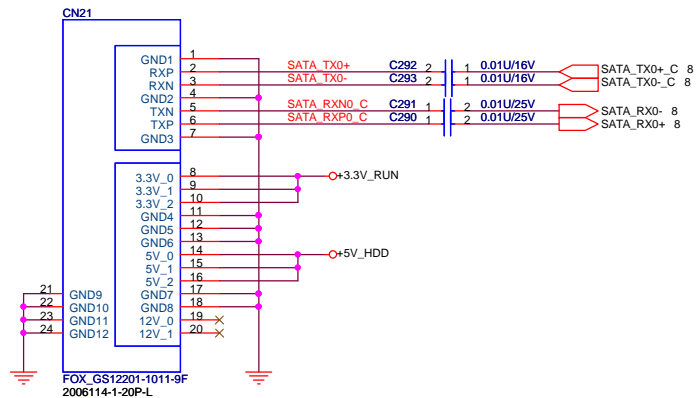
TV module



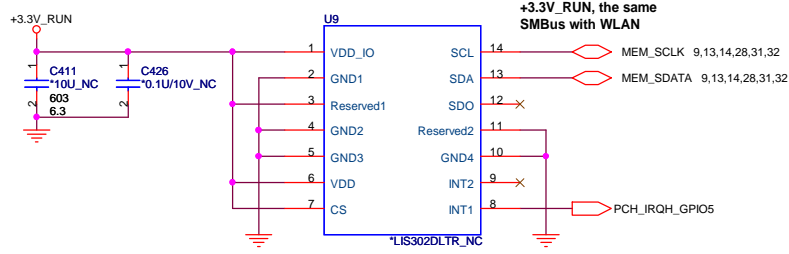
TV RF Jack & Microwave connector



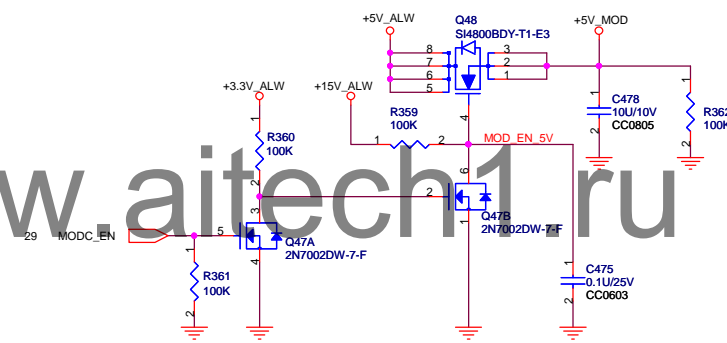
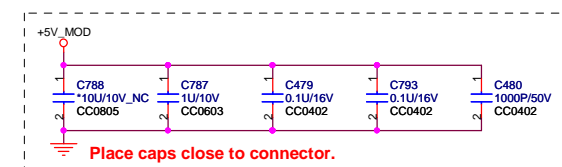
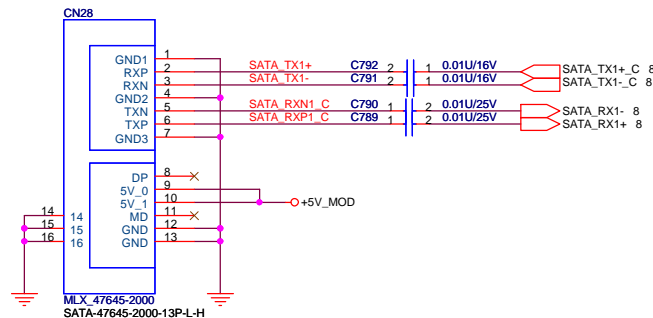
## SATA Connector



## 3-axis Fall Sensor (HDD data protector)



## ODD Connector



Title			HDD & ODD (SATA)
Size	Document Number	Rev	
	RM5C	B1B	
Date:	Friday, October 23, 2009	Sheet	34 of 60



## To Daughter Board connector

Solid White = System On, Normal Activity  
Off= System off (system off or hibernated);  
"Breathing White" = System in Standby (S3);

### Power Button

### Speaker

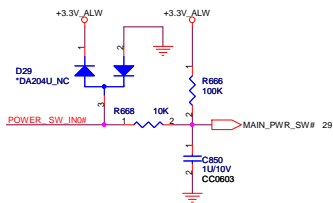
### KB LED

### Touch Pad

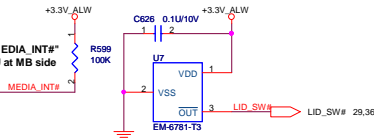
### Media Button

Scott\_0123: Change CN8 PN with DFHD32MR003 (With mylar)

### Power Button



### Hall Switch

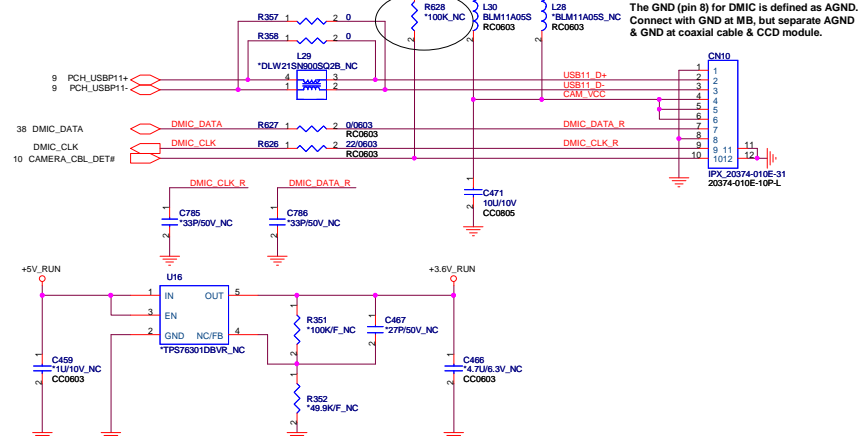


### Active high for ISSP reset

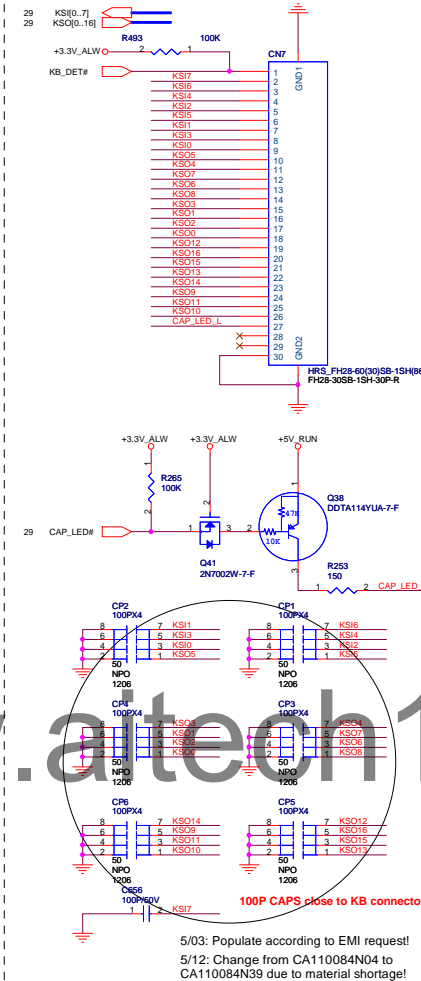


## Array Microphone & Camera

1007 for change list



## KEYBOARD CONNECTOR



5/03: Populate according to EMI request!

5/12: Change from CA110084N04 to CA110084N39 due to material shortage!



File	KB/ CCD/ UI
Size	Document Number RMSC
Date	Friday, October 23, 2009
Sheet	35 of 60
Rev	818

## Hinge & Power Button board LED (PWR/Battery indicator)

### Hinge LED

Solid White= System On, Normal Activity  
Solid White= Charging (system on);  
Solid White= Charging (system off or hibernate and battery charge <90%);  
Off= Charging (system off or hibernate and battery charge > 90%);  
"Breathing White " = System in Standby (S3);  
Off = System Off (or in Hibernate);

Scott\_0912: Change to +5V\_ALW power rail for solve LED blinking issue.

### Power button board LED:

Solid White = System On, Normal Activity  
Off= System off (system off or hibernate);  
"Breathing White " = System in Standby (S3)

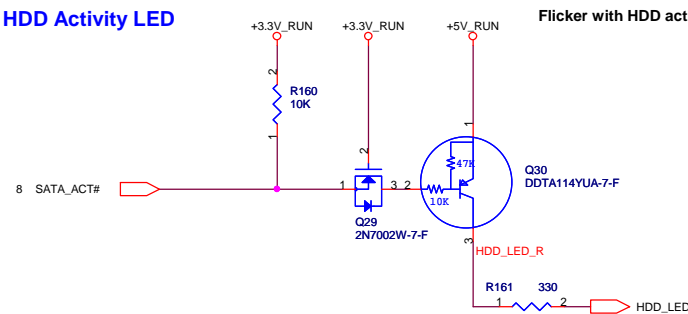
### Hinge LED:

Flashing Amber = Low Battery (S0 and S3 and no AC) when battery charge <10%  
Flash rate = on 1/4 sec., off 3/4 sec.

www.aitech1.ru

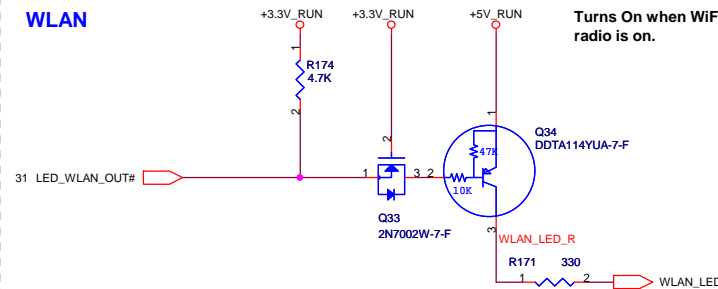
## HDD Activity LED

Flicker with HDD activity.



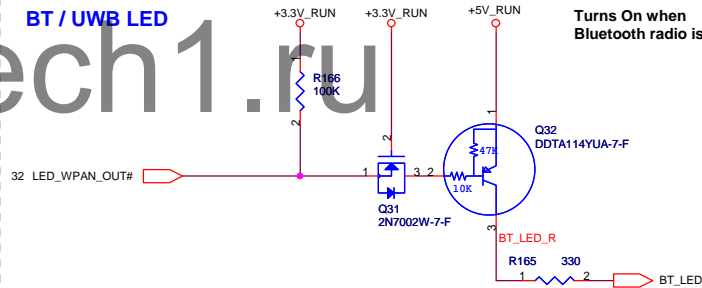
## WLAN

Turns On when WiFi radio is on.



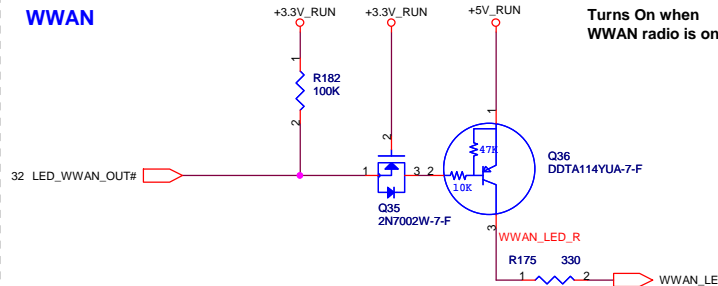
## BT / UWB LED

Turns On when Bluetooth radio is on.



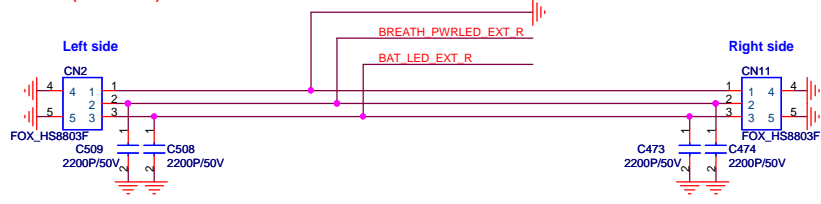
## WWAN

Turns On when WWAN radio is on.



## Hinge LED (PWR/Battery indicator)

L-C filter (reserve R-C) for EMI

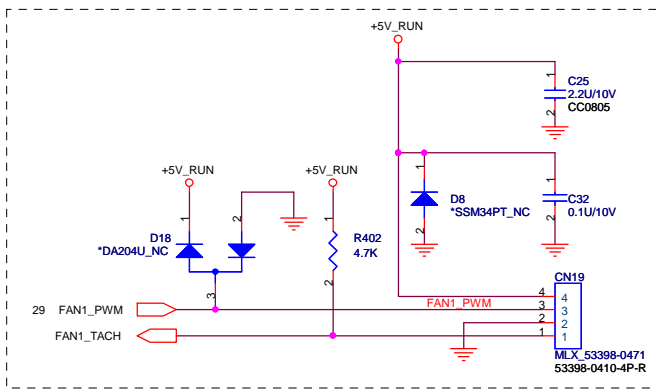


Solid White= System On, Normal Activity  
Solid White= Charging (system on);  
Solid White= Charging (system off or hibernate and battery charge <90%);  
Off= Charging (system off or hibernate and battery charge > 90%);  
"Breathing White " = System in Standby (S3);  
Off = System Off (or in Hibernate);

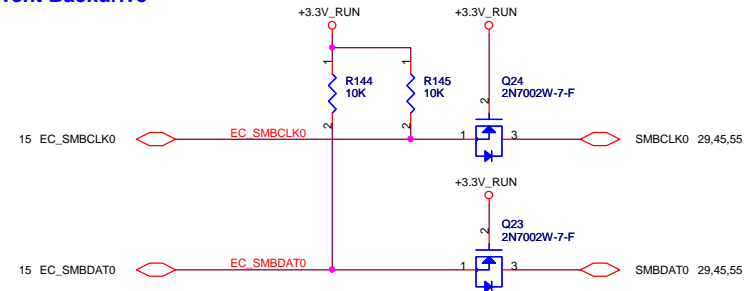
Flashing Amber = Low Battery (S0 and S3 and no AC) when battery charge <10%  
Flash rate = on 1/4 sec., off 3/4 sec.



Title		
LED		
Size	Document Number	Rev
	RMSC	B1B
Date:	Friday, October 23, 2009	Sheet 36 of 60

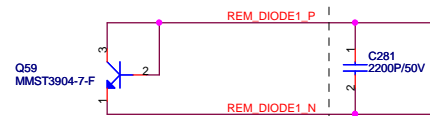


### Prevent Backdrive



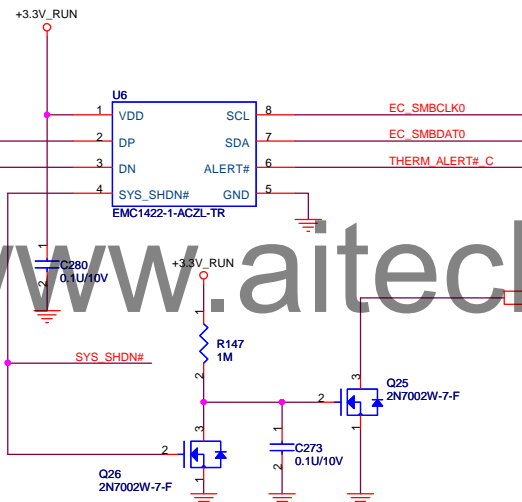
Place these under CPU

10/20mils

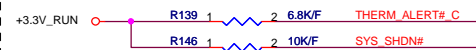


1. Place C579 close to EMC1422  
Total capacitance between D+/D- is 2200pF(max)

www.aitech1.ru



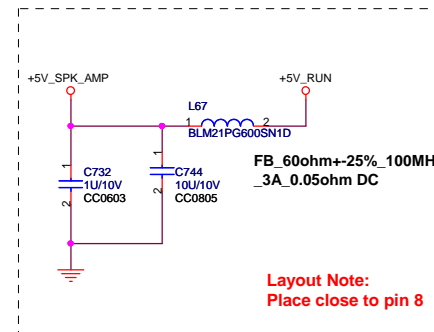
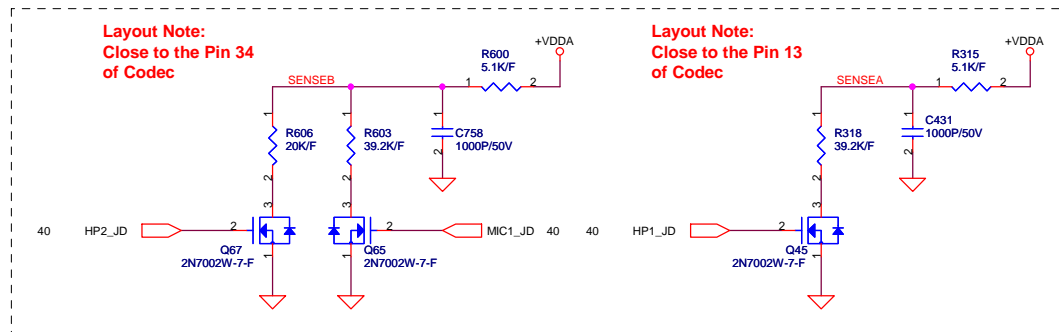
OTP 90 degree



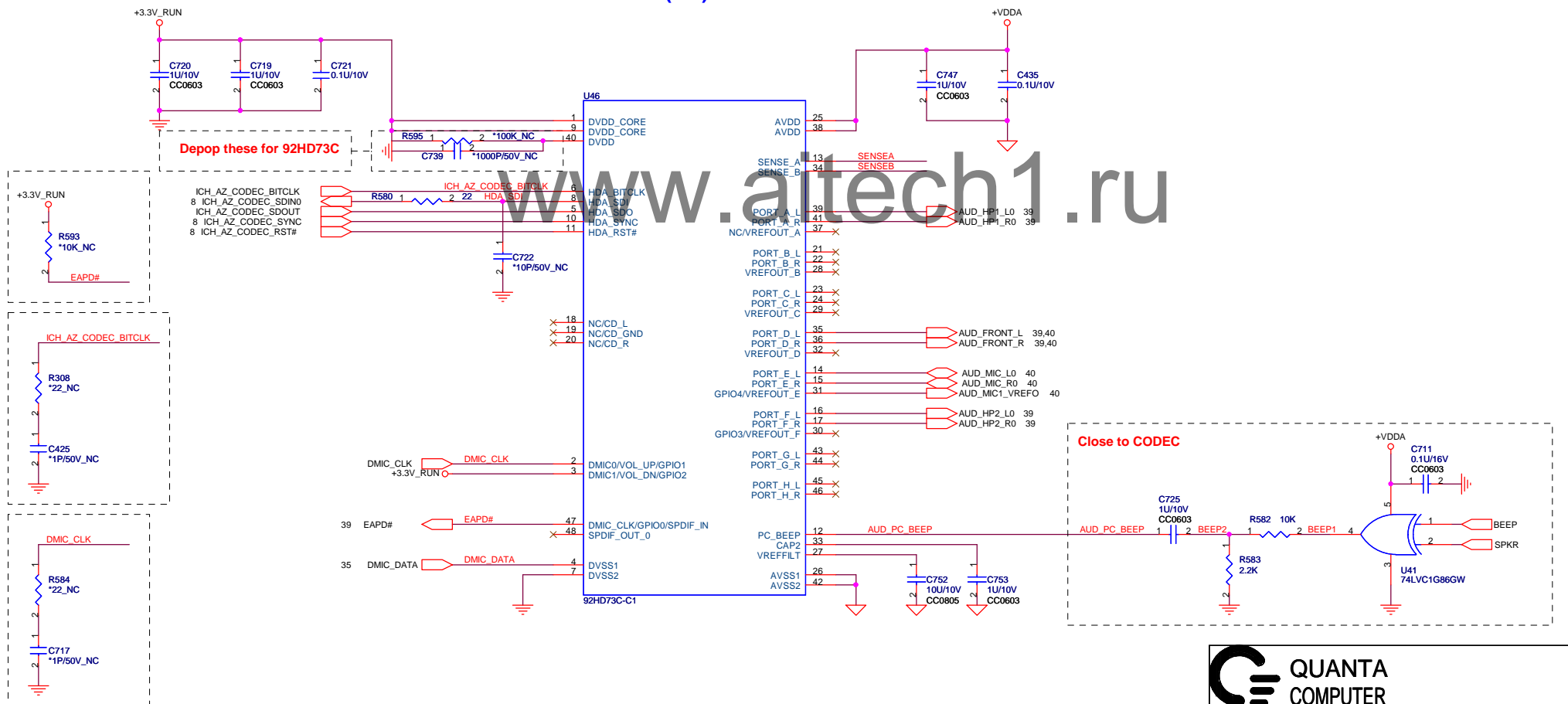
OTP 85 degree : R98 = 10K, R103 = 6.8K  
OTP 90 degree : R98 = 6.8K, R103 = 10K



Title			FAN /THERMAL
Size	Document Number	Rev	
	RM5C	B1B	
Date:	Friday, October 23, 2009	Sheet	37 of 60

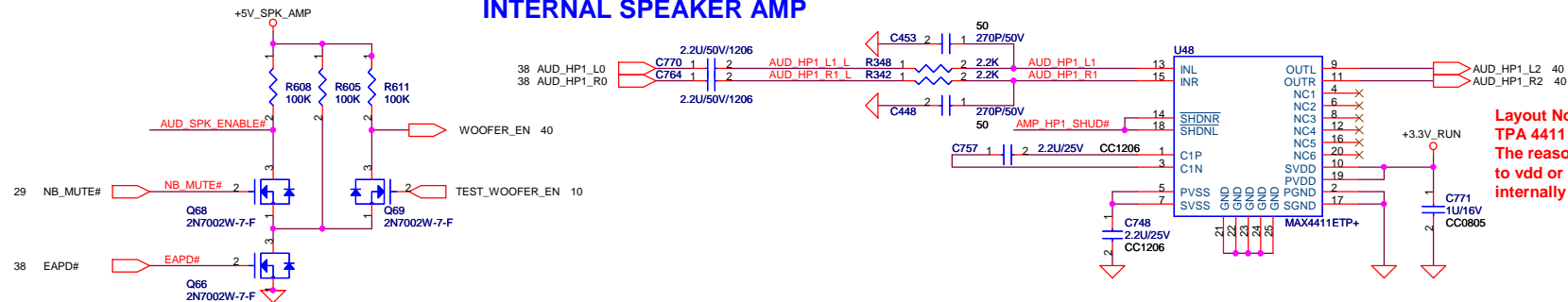


## AZALIA (HD) CODEC

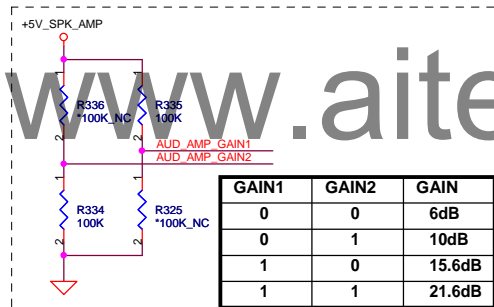
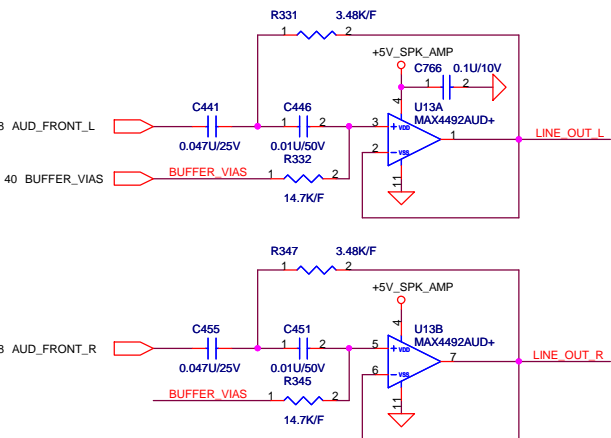
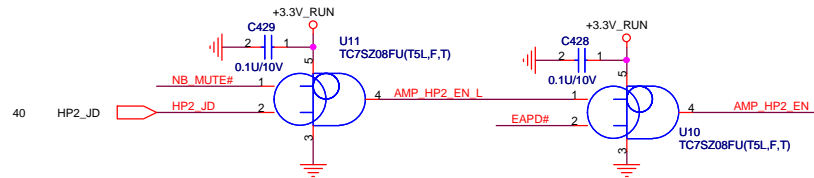
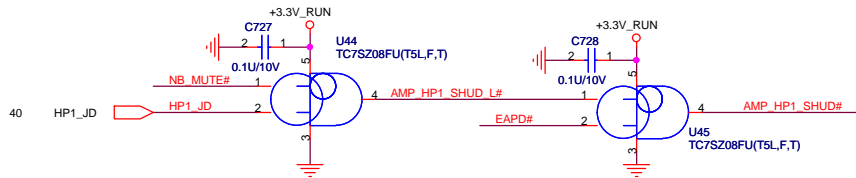


Title			AZELIA CODEC (92HD73C)
Size	Document Number	Rev	
	RMSC	B1B	
Date:	Friday, October 23, 2009	Sheet	38 of 60

# INTERNAL SPEAKER AMP

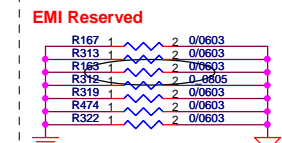
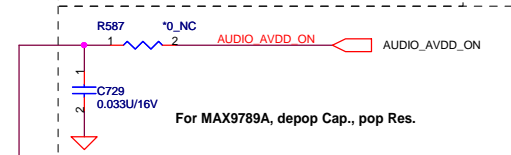


**Layout Note:**  
TPA 4411 : cannot connect EP to GND.  
The reason that we can't solder the pad to vdd or ground is because it is internally connected to VSS.

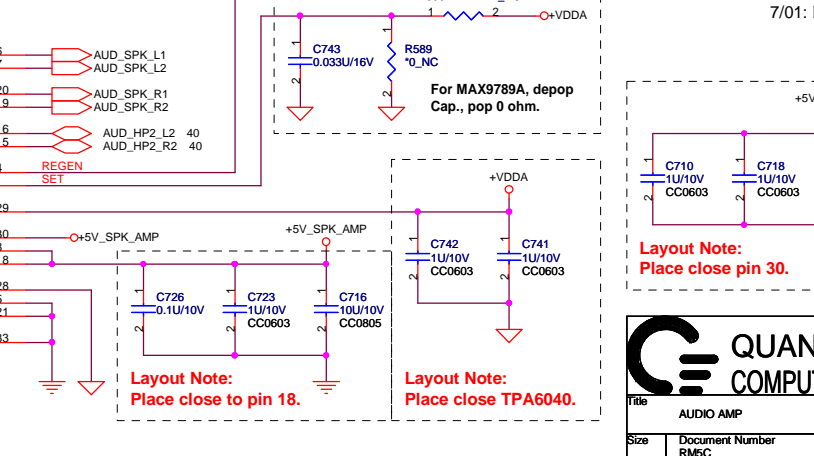
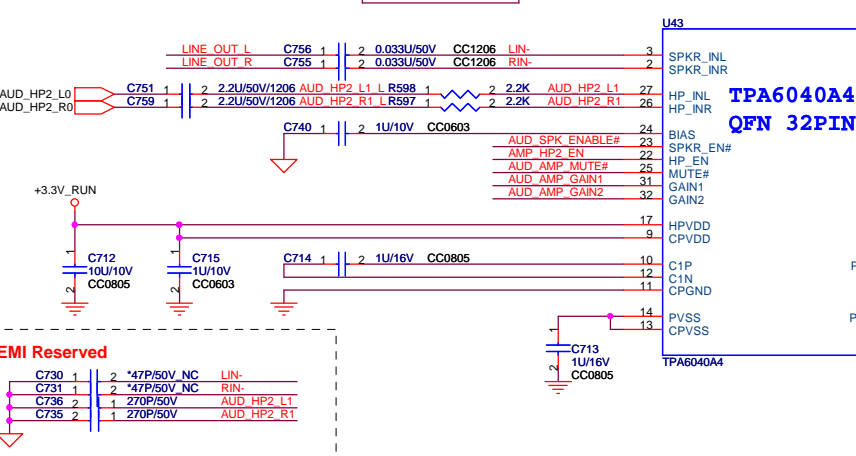


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

**Layout Note:**  
MAX9789A/TPA6040A : need to connect EP (exposed paddle) to GND.  
TPA 4411 : cannot connect EP to GND.  
MAX 4411 : can connect EP to GND.

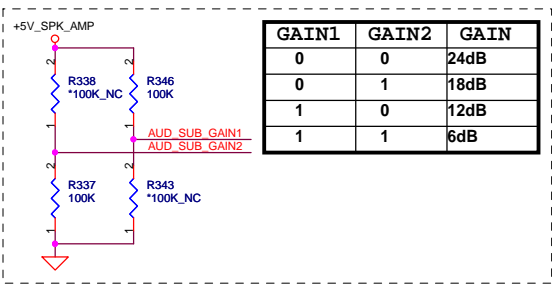
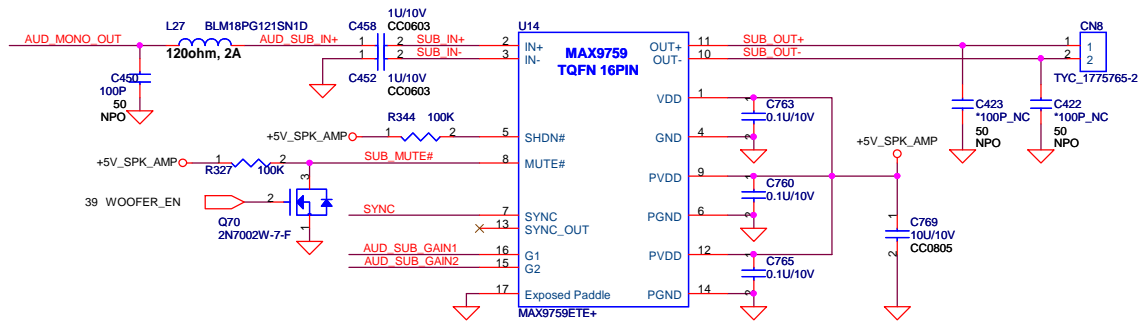
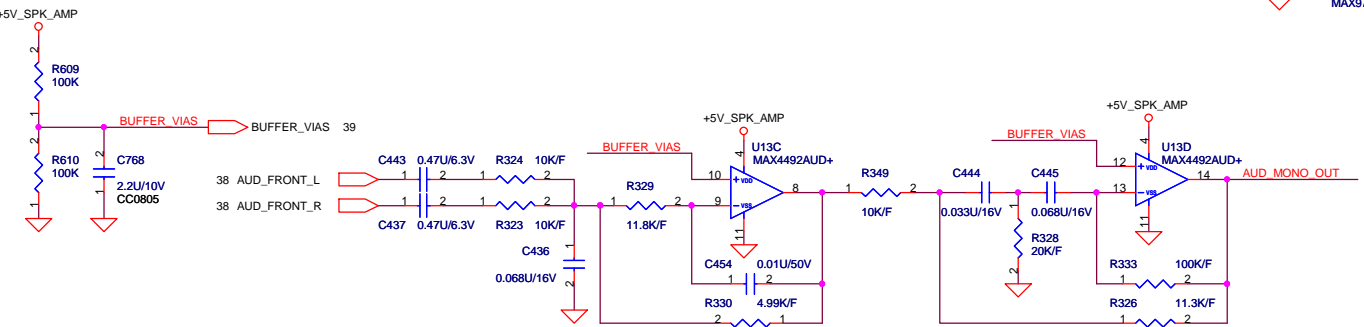
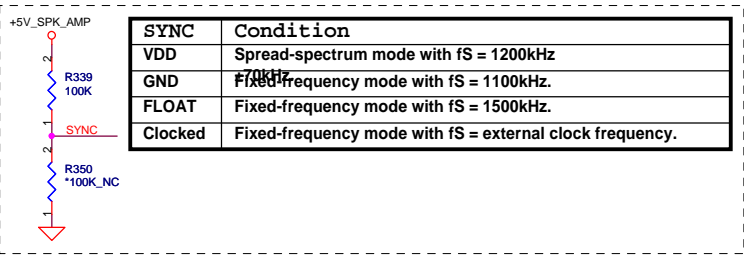


7/01: Populate according to EMI request!

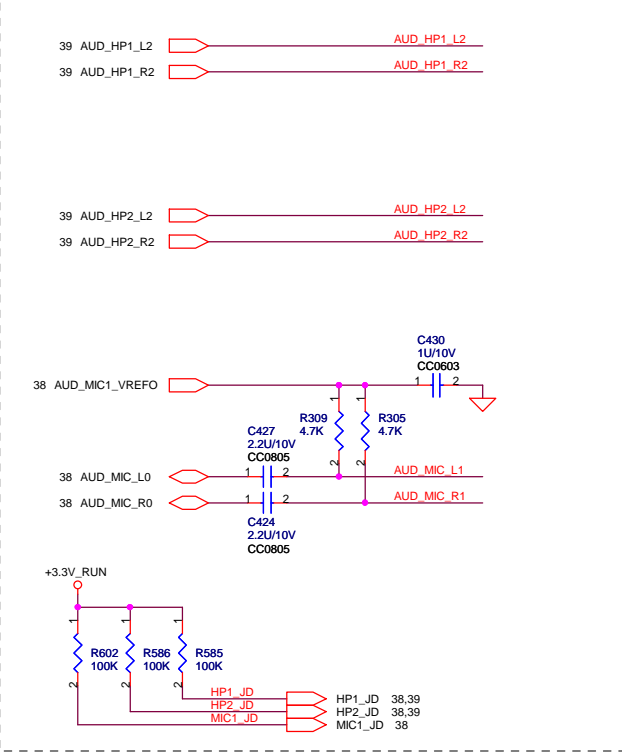


Title		
AUDIO AMP		
Size	Document Number	Rev
	RMSC	B1B
Date:	Friday, October 23, 2009	Sheet 39 of 60

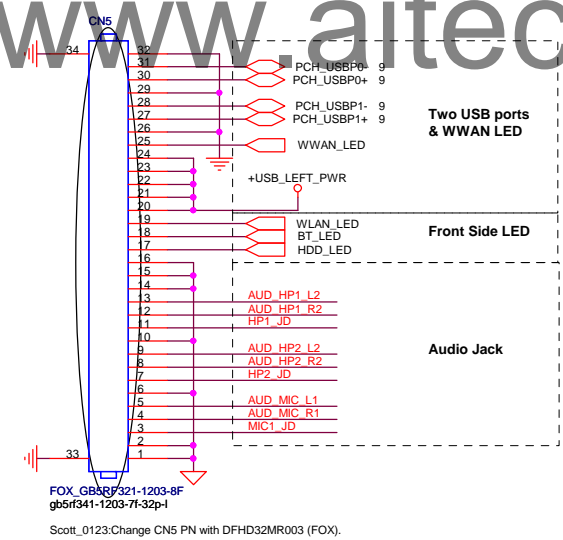
INTERNAL SUBWOOFER AMP



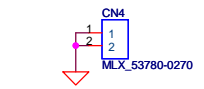
Ambient Parts of Headphone & MIC Jack



To IB(IO Board) connector



Adding additional AGND

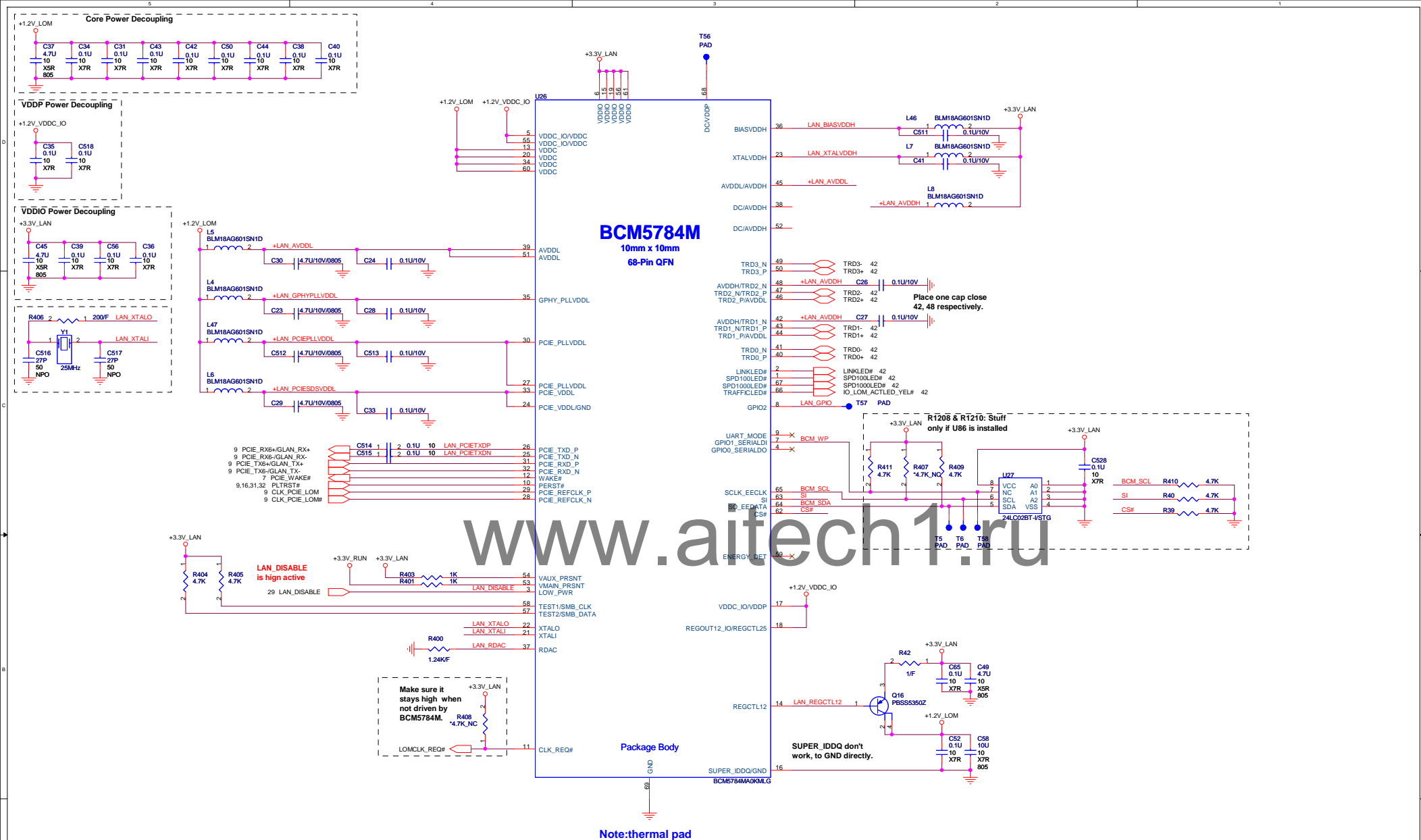


QUANTA COMPUTER logo and title: IB CONN & SUBWOOFER

Size: Document Number RMSC Rev B1B

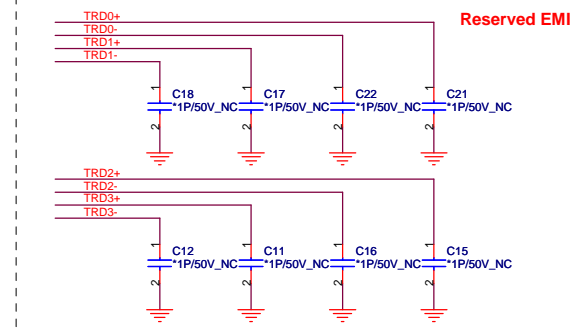
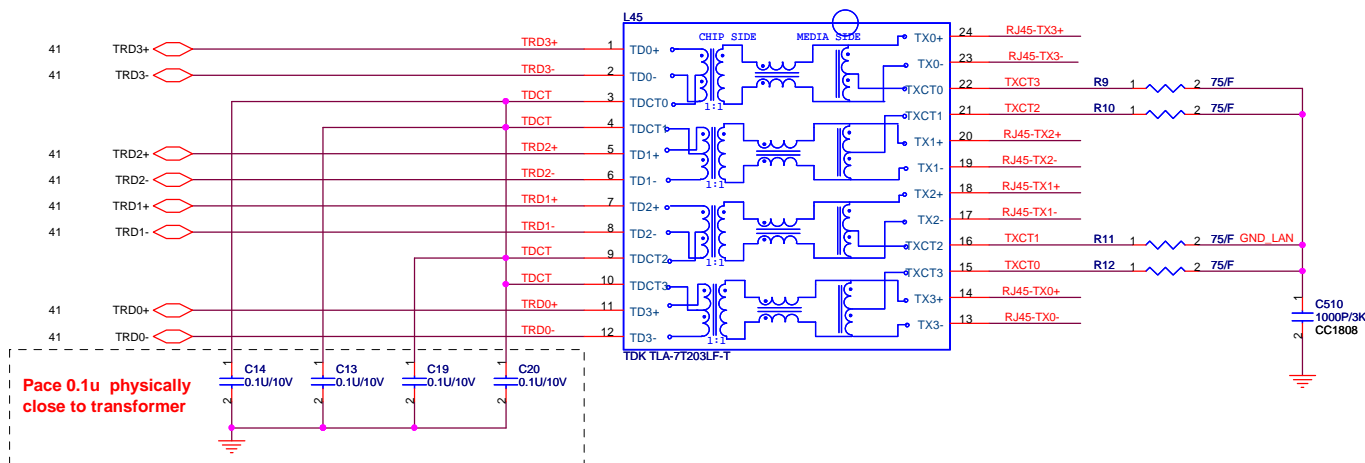
Date: Friday, October 23, 2009 Sheet 40 of 60



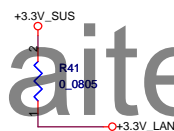
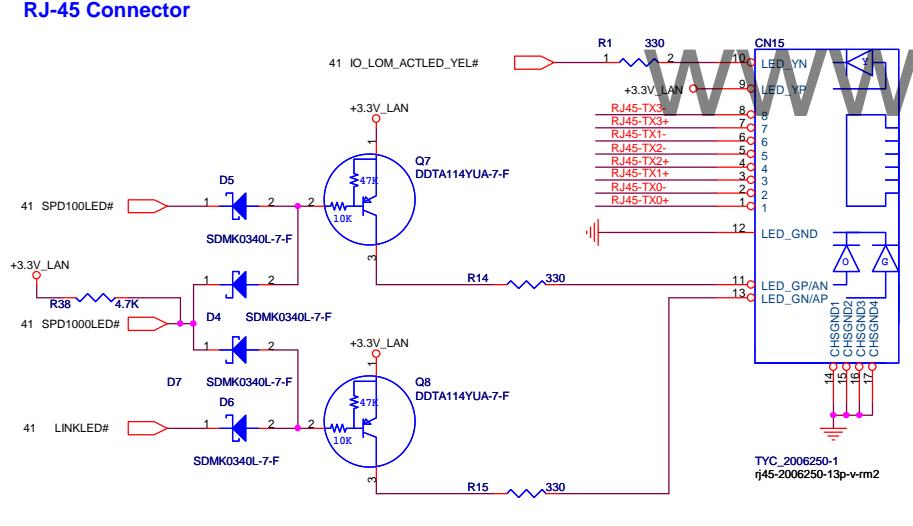


## TRANSFORMER

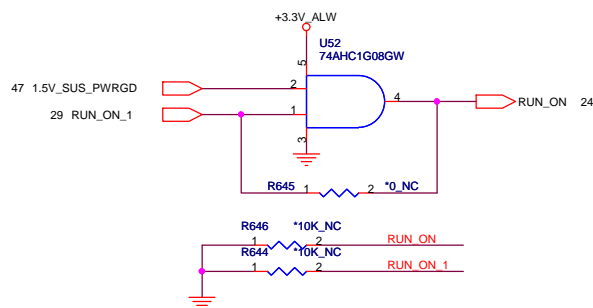
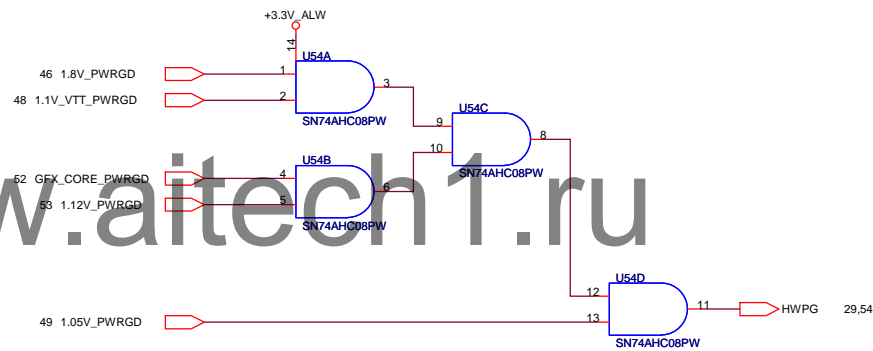
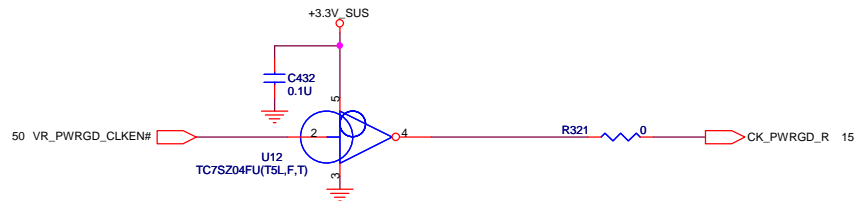
**Layout Note:**  
Route TRD+/- pairs with 100 ohm differential trace impedance.



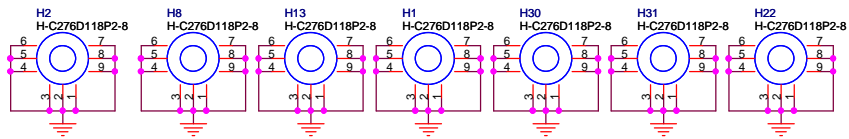
## RJ-45 Connector



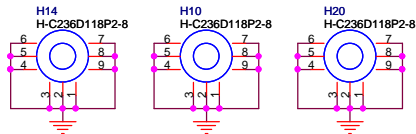
Title			LAN SWITCH
Size	Document Number	Rev	
	RMSC	B1B	
Date:	Friday, October 23, 2009	Sheet	42 of 60



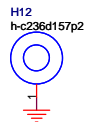
H-C276D118P2-8 \* 7



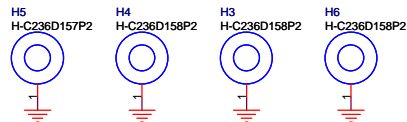
H-C236D118P2-8 \* 3



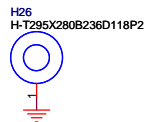
h-c236d197p2 \* 1



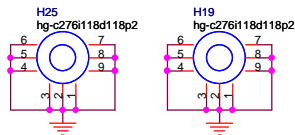
H-C236D158P2 \* 4



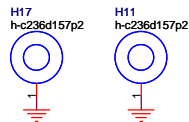
H-T295X280B236D118P2 \* 1



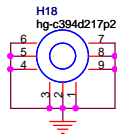
hg-c276i118d118p2 \* 2



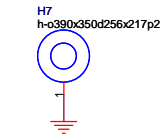
h-c236d157p2 \* 2



h-c394d260p2 \* 1



H-C394D260P2-8 \* 1



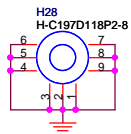
Scott\_0731: change H7 & H18 footprint as ME change

Scott\_0812:Delete H7 Pin2~Pin9 for layout requite.

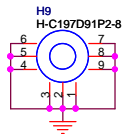
h-c236d236n \* 2



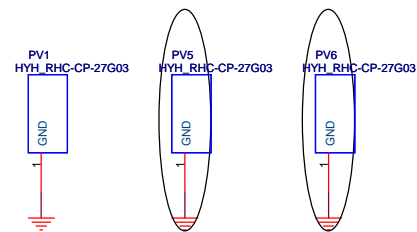
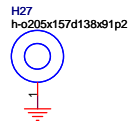
H-C197D118P2-8 \* 1



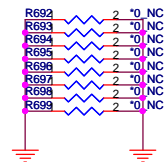
H-C197D91P2-8 \* 1



h-o205x157d138x91p2 \* 1



Scott\_0701:: Added PV6 according to EMI's suggestion



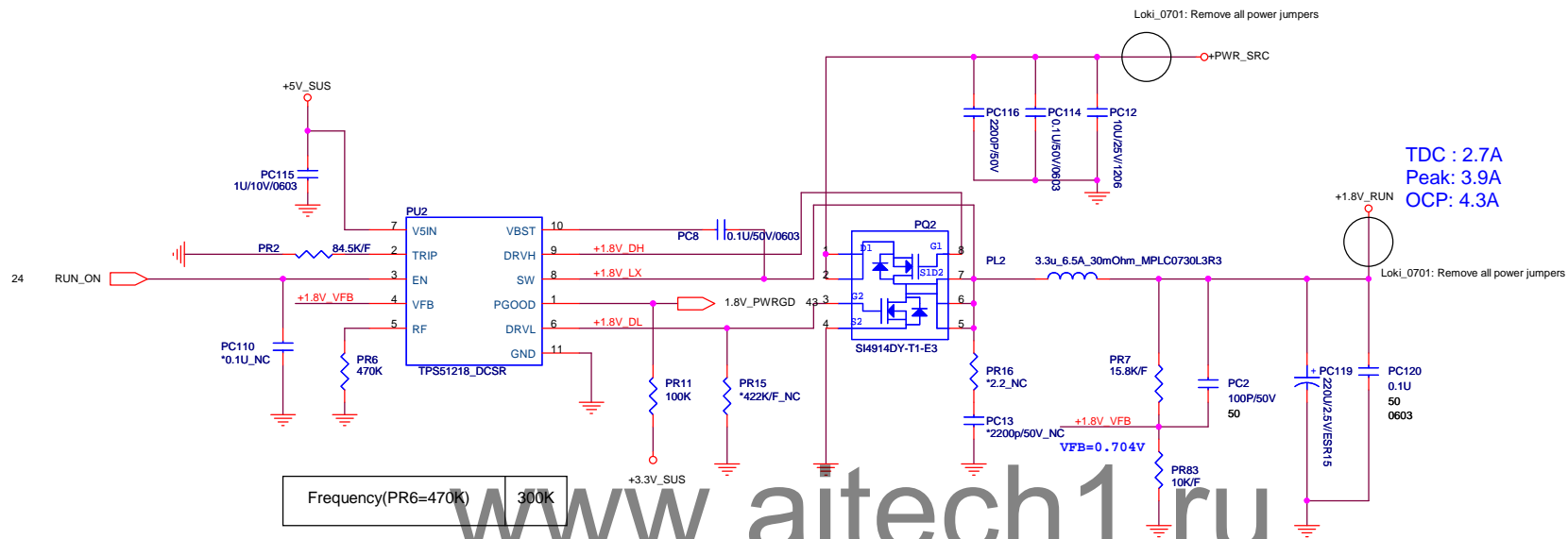
Scott\_0703:Add 8pcs 0ohm resistors R692~R699 for thermal issue as EMI concern.

Scott\_0707: Reserver R692~R699.



www.aitech1.ru



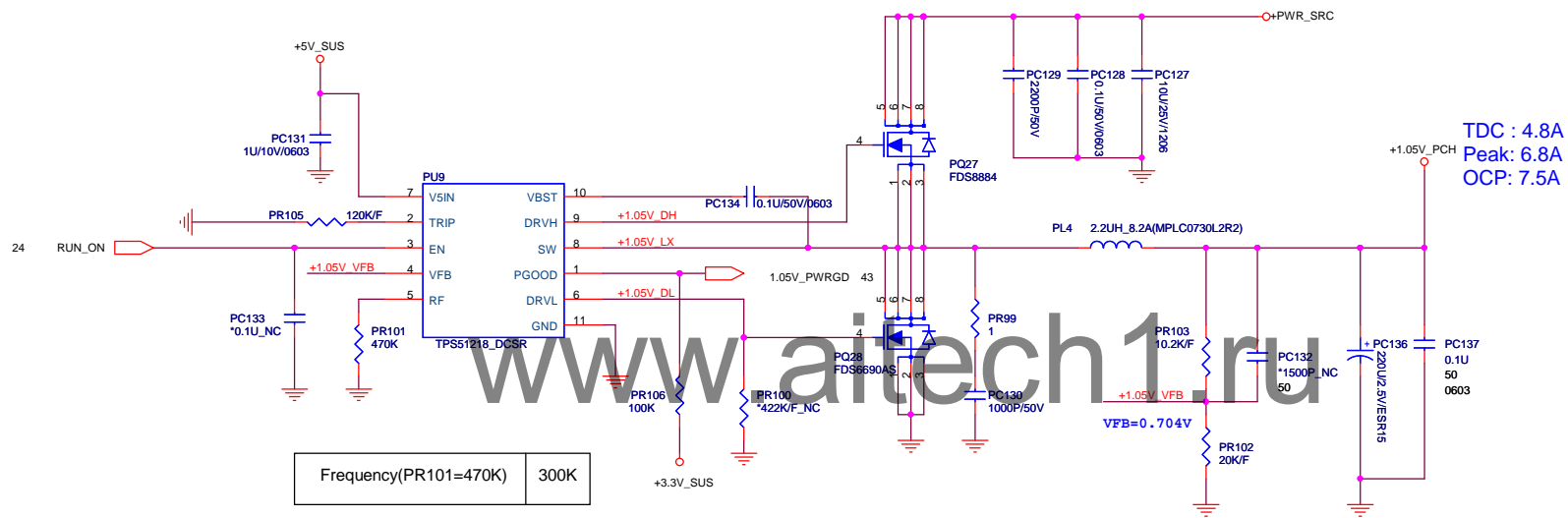


Title		
+1.8V_RUN (TPS51218)		
Size	Document Number	Rev
	RMSC	B1B
Date:	Friday, October 23, 2009	Sheet 46 of 60

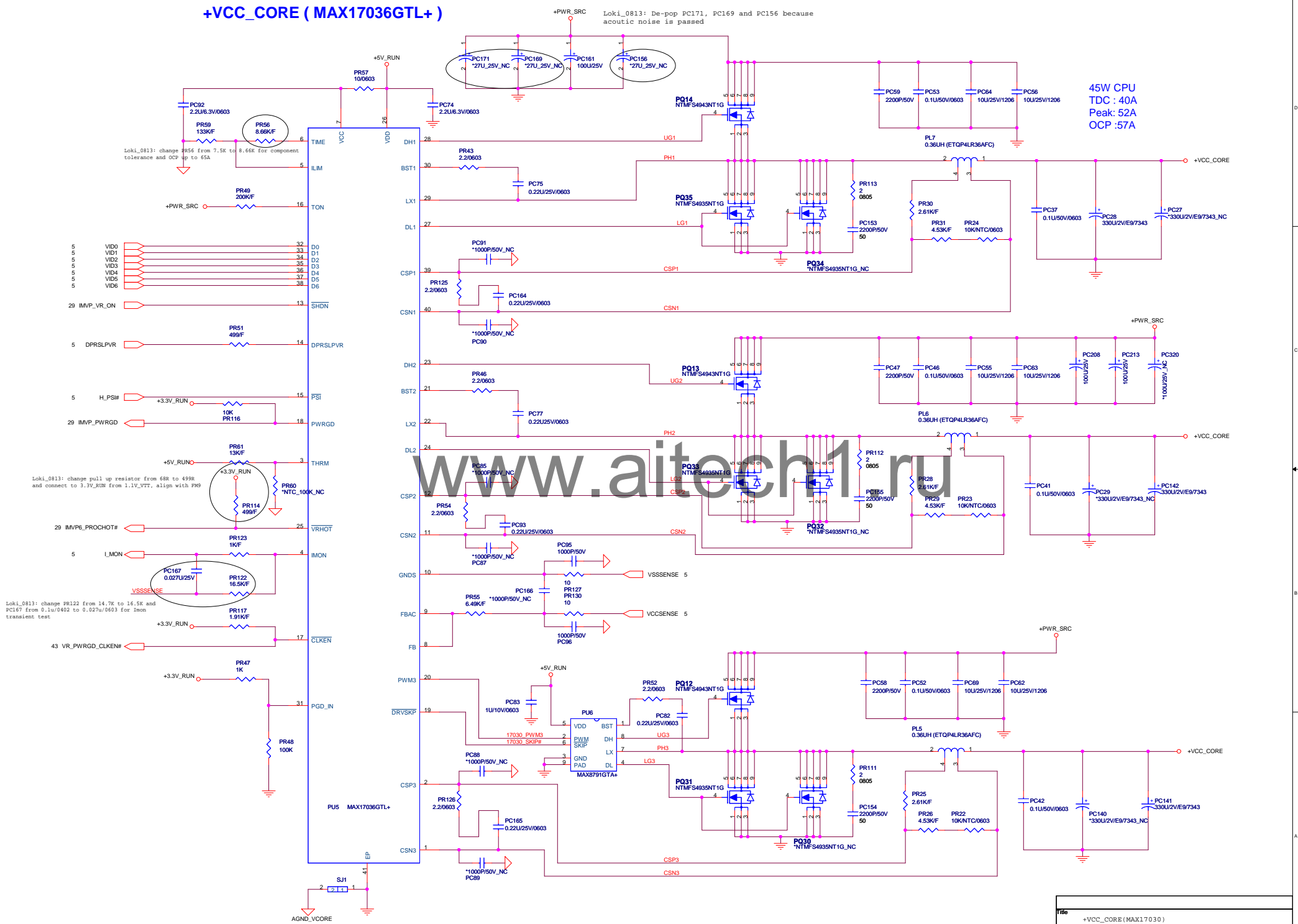


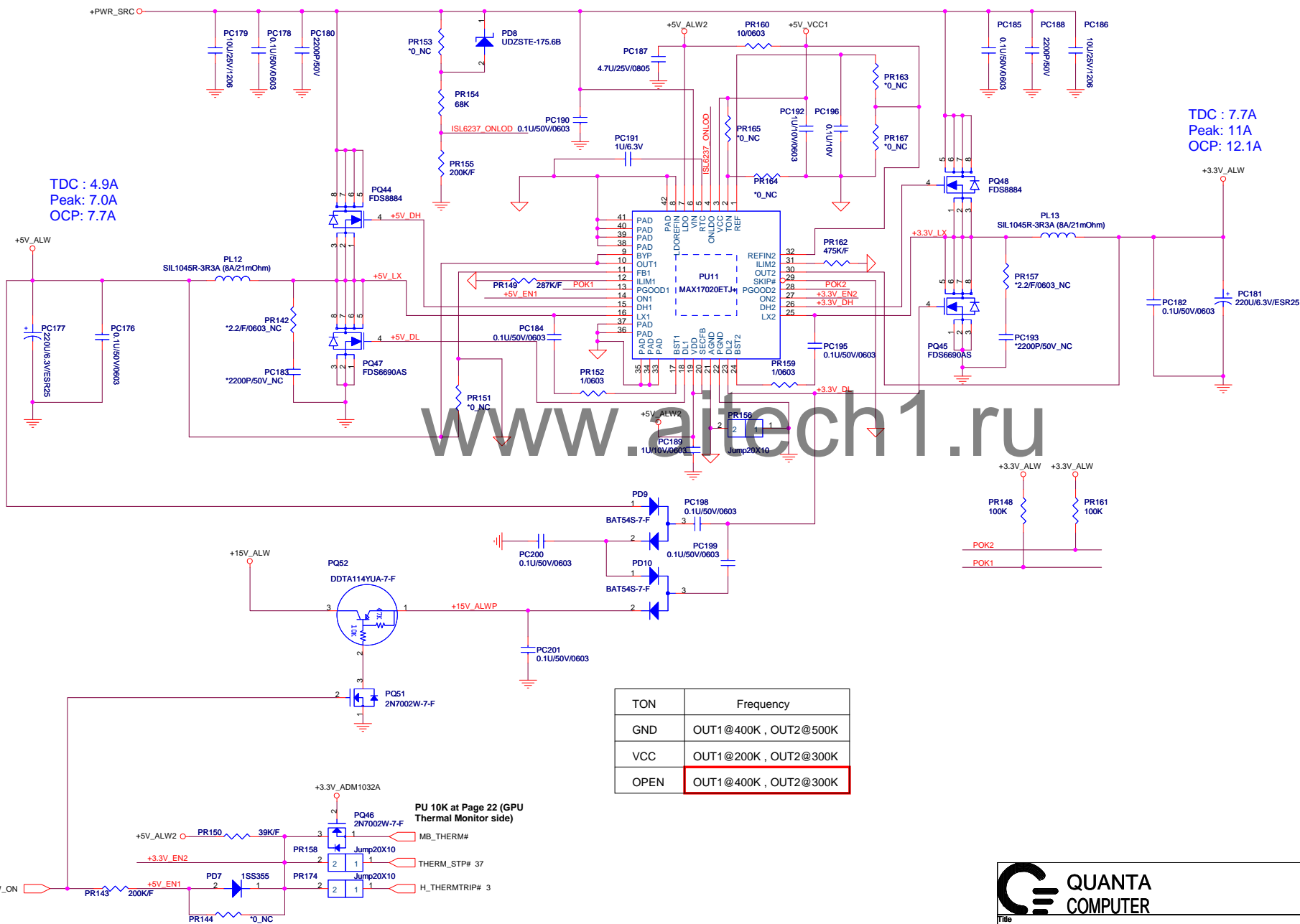






# +VCC\_CORE ( MAX17036GTL+ )





TDC : 7.7A  
Peak: 11A  
OCP: 12.1A

TDC : 4.9A  
Peak: 7.0A  
OCP: 7.7A

TON	Frequency
GND	OUT1@400K , OUT2@500K
VCC	OUT1@200K , OUT2@300K
OPEN	OUT1@400K , OUT2@300K

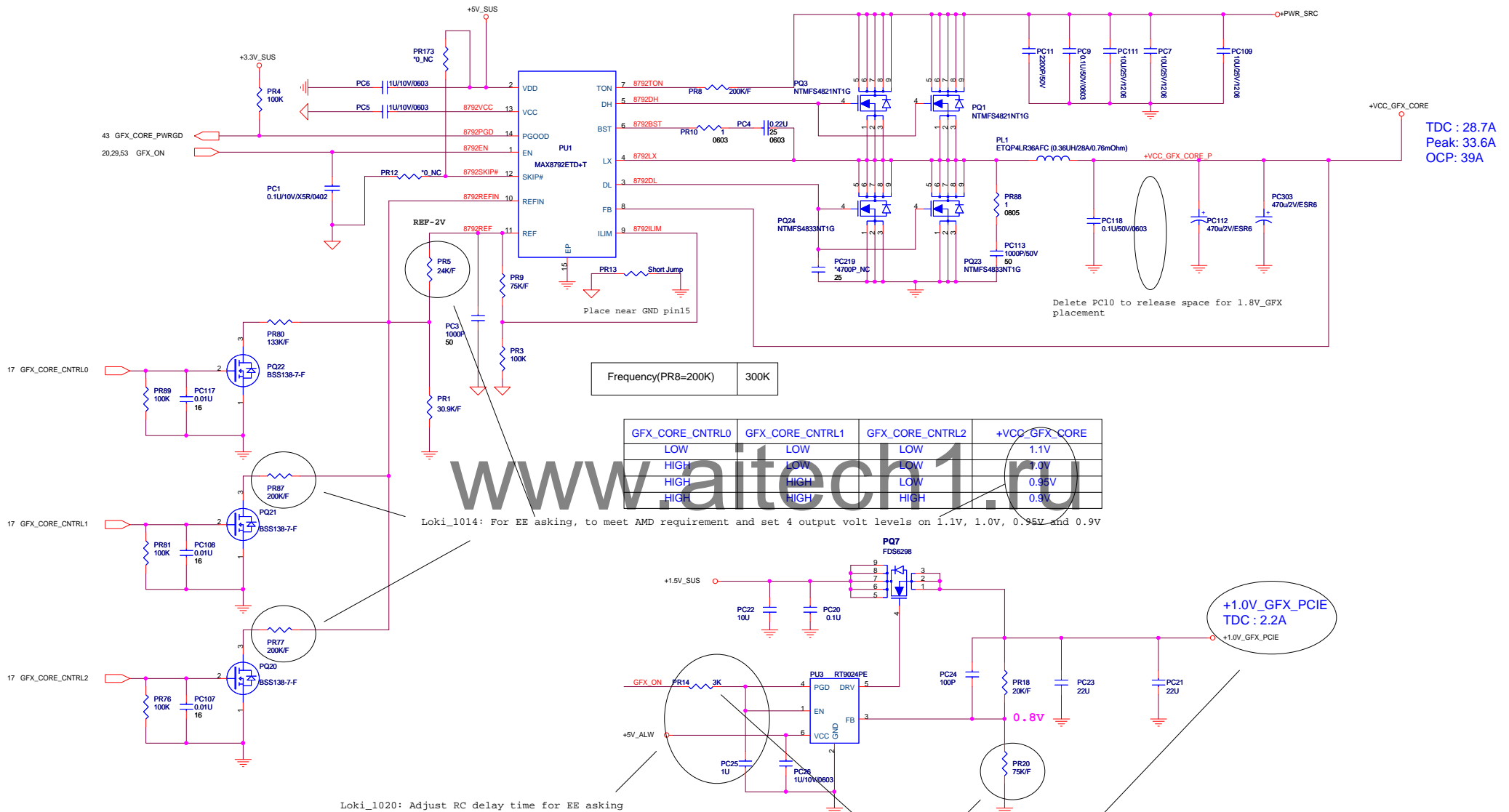
PU 10K at Page 22 (GPU Thermal Monitor side)

**QUANTA COMPUTER**

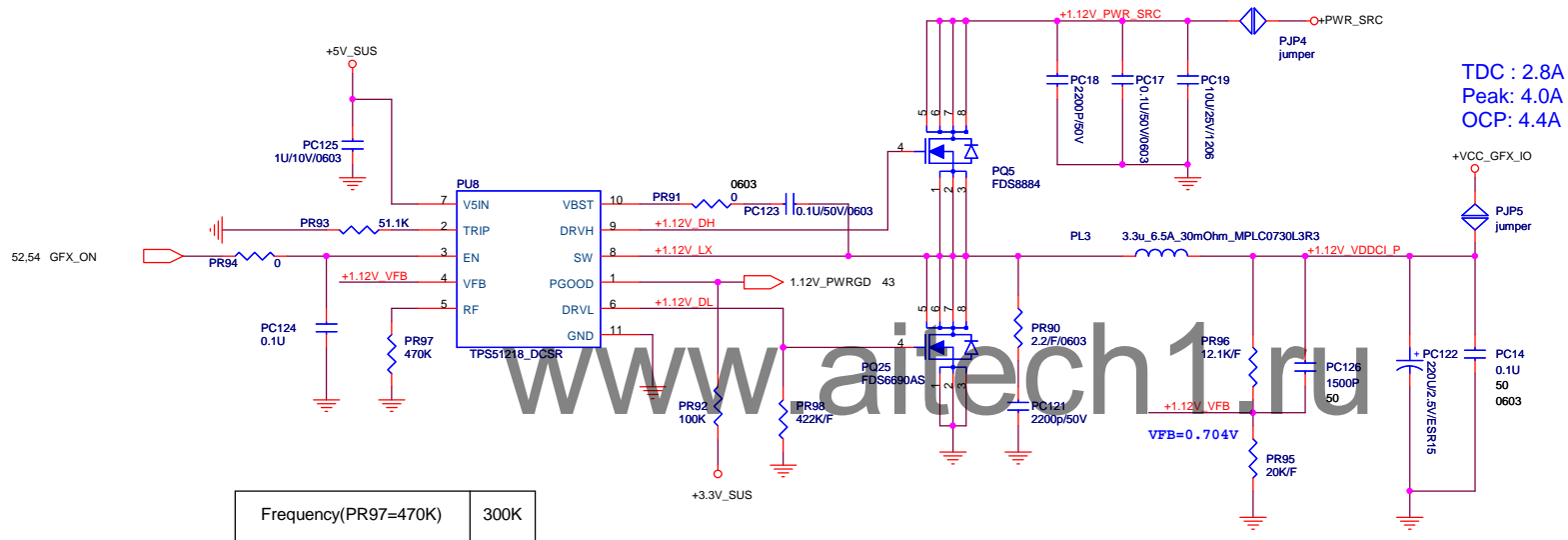
Title: +3.3V/+5V/+15V (MAX17020)

Size: Document Number RM5C Rev B1B

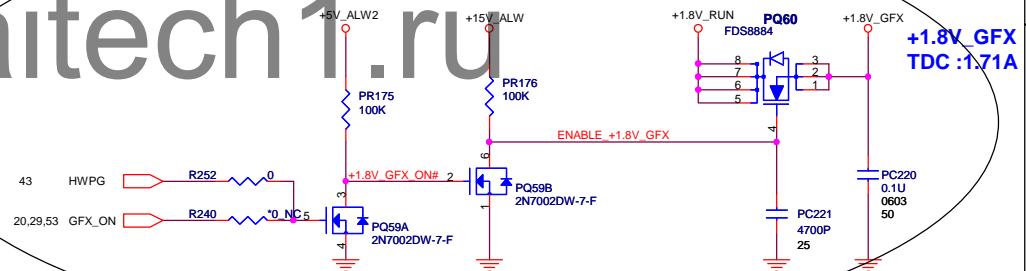
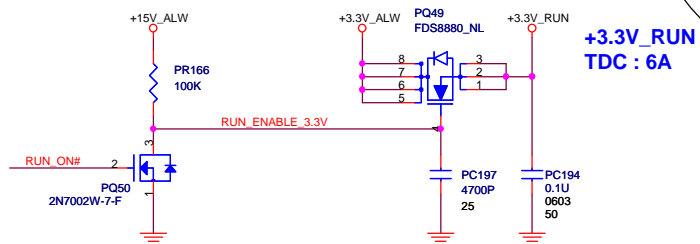
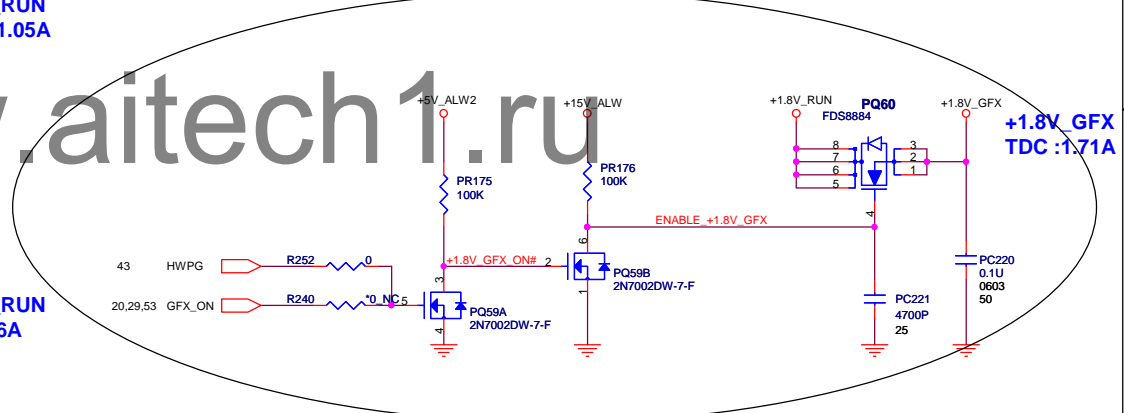
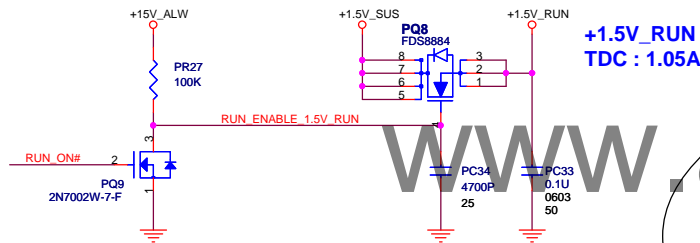
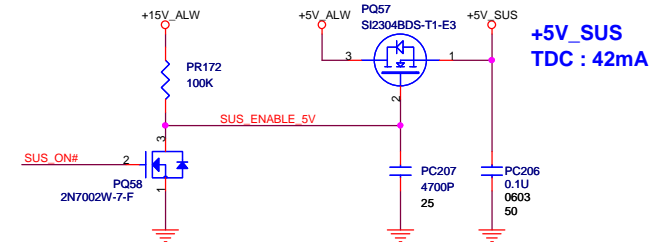
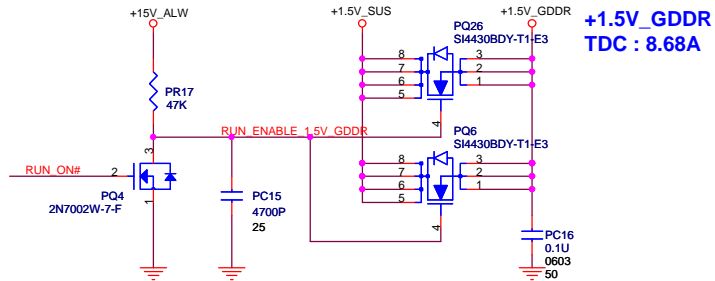
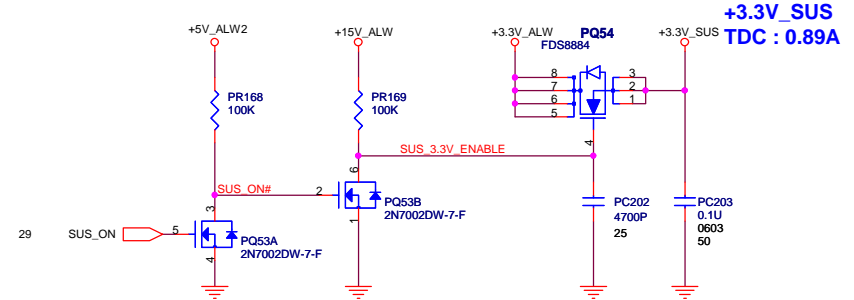
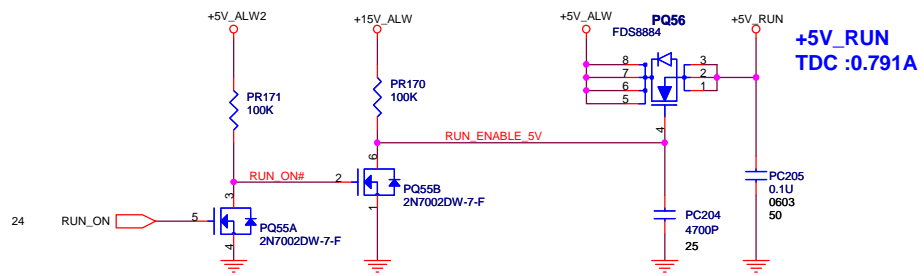
Date: Friday, October 23, 2009 Sheet 51 of 60





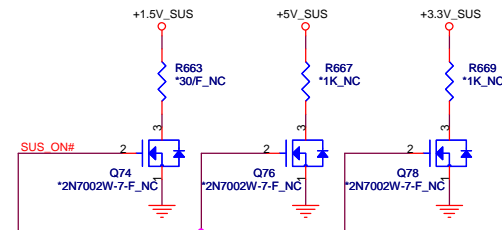
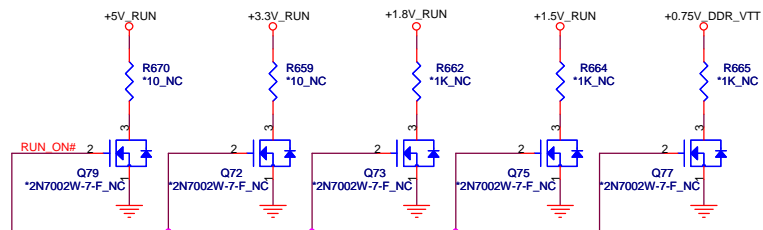


Title		
+VDDCI_M97 (TPS51218)		
Size	Document Number RMS	Rev B1B
Date:	Friday, October 23, 2009	Sheet 53 of 60

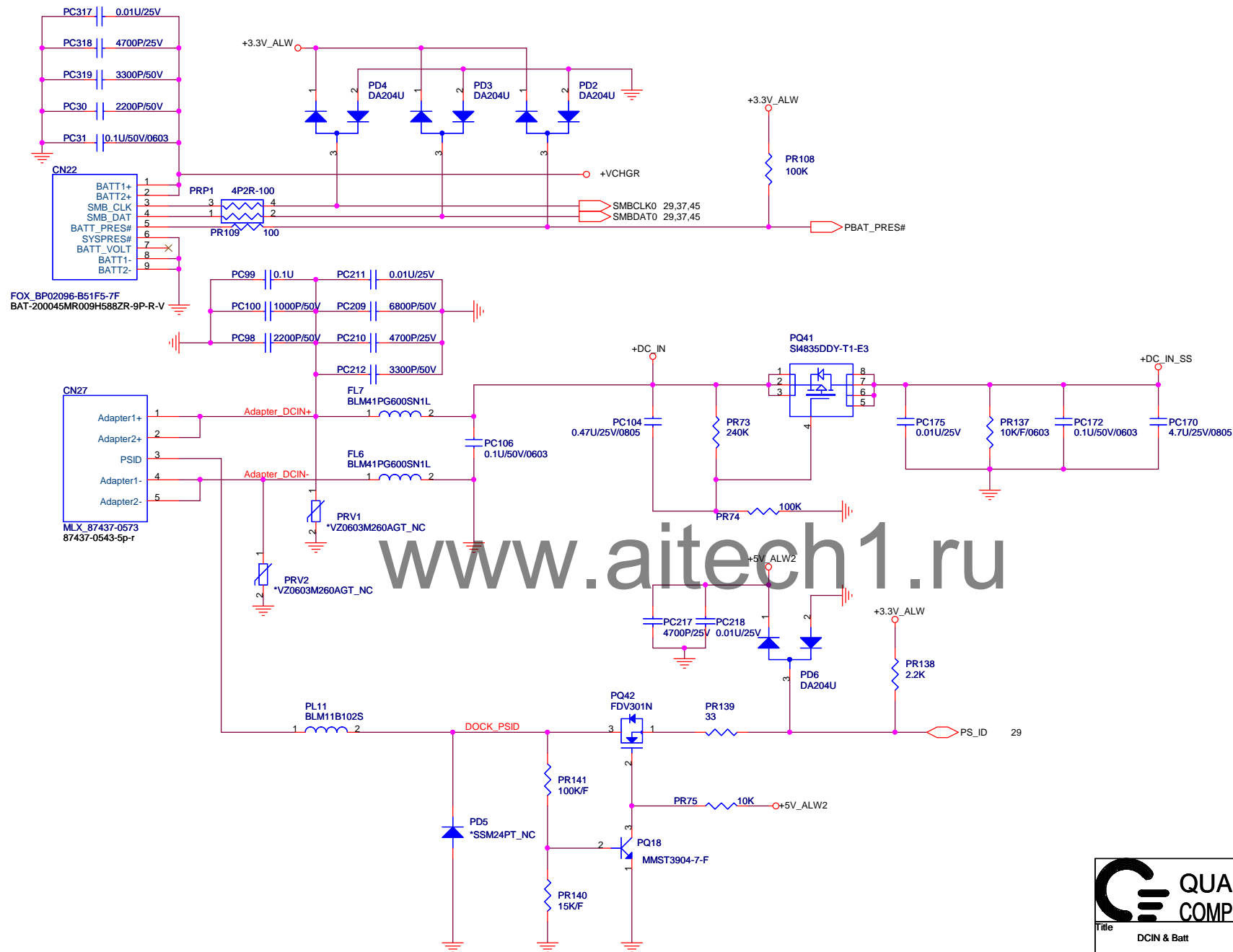


Loki\_1014: For EE asking, to separate +1.8V\_RUN and +1.8V\_GFX power rail

### Reserve discharge path



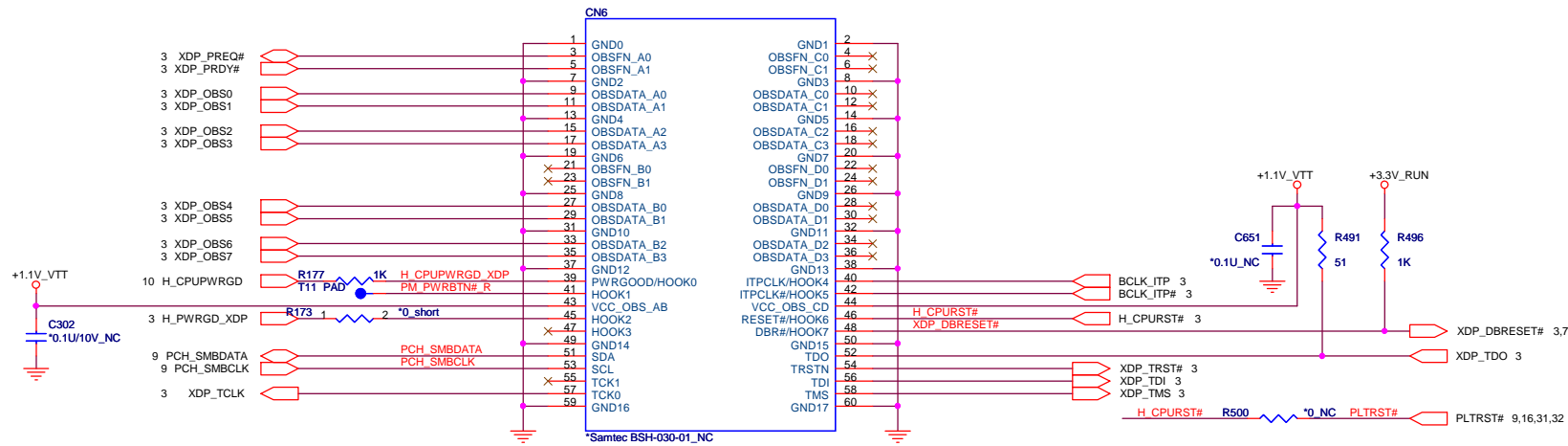
Title: RUN POWER SW		
Size: Document Number	Rev: B1B	
Date: Friday, October 23, 2009	Sheet: 54	of: 60



Title	DCIN & Batt
-------	-------------

Date: Friday, October 23, 2009

## CPU XDP

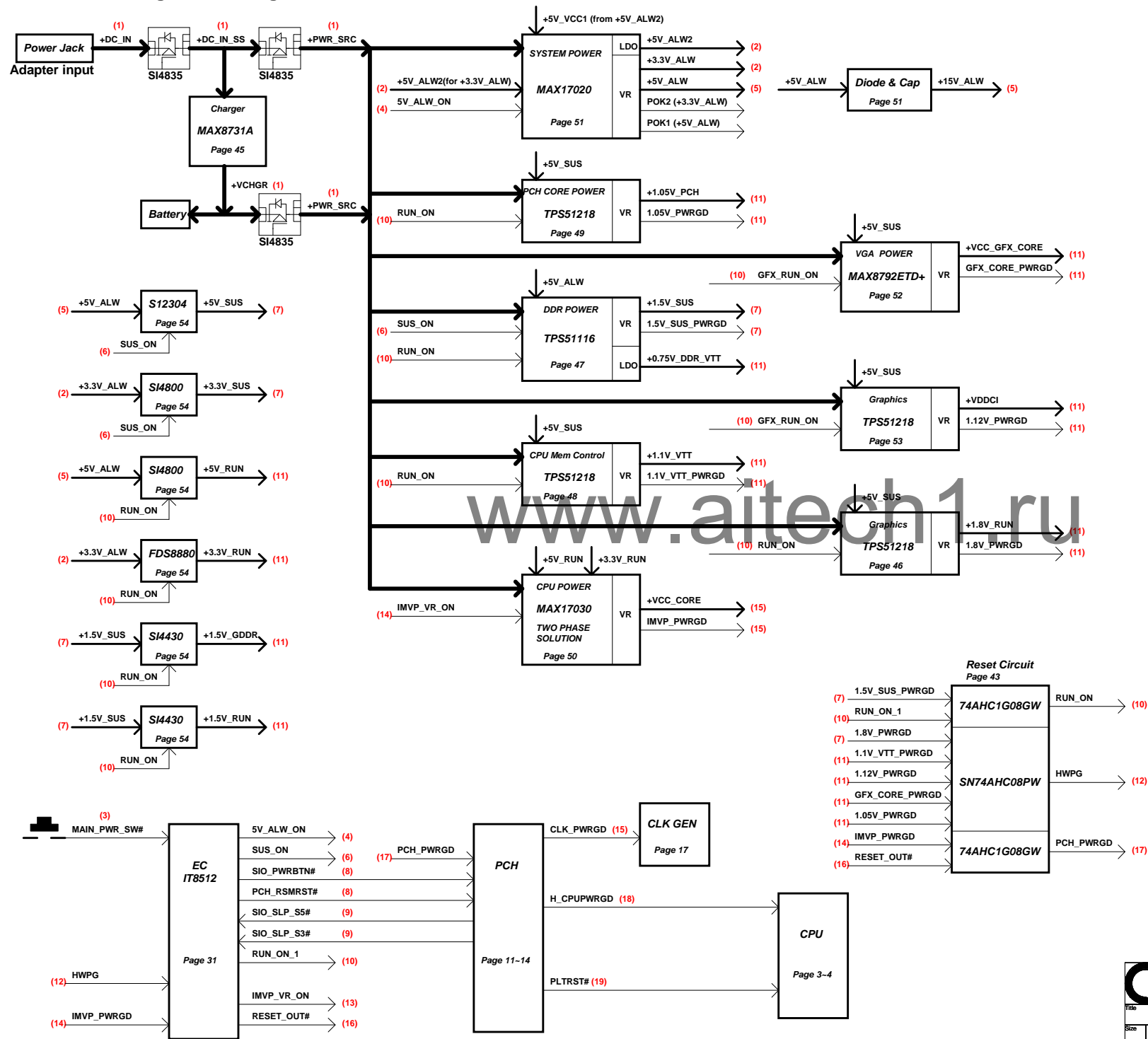


## PCH XDP

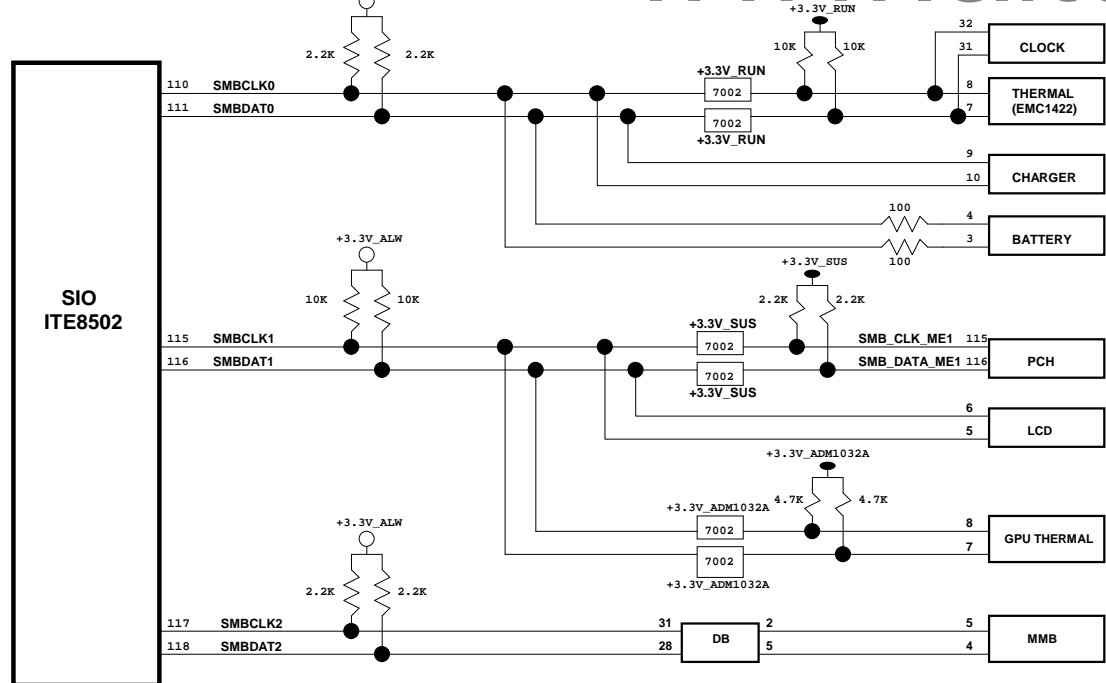
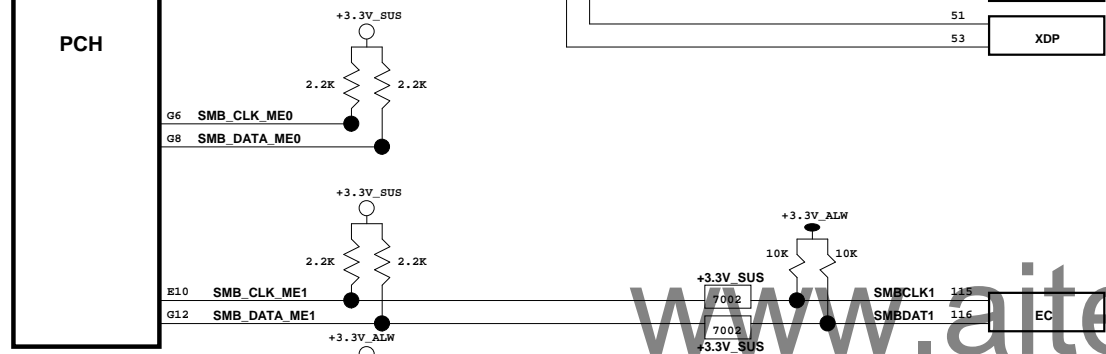
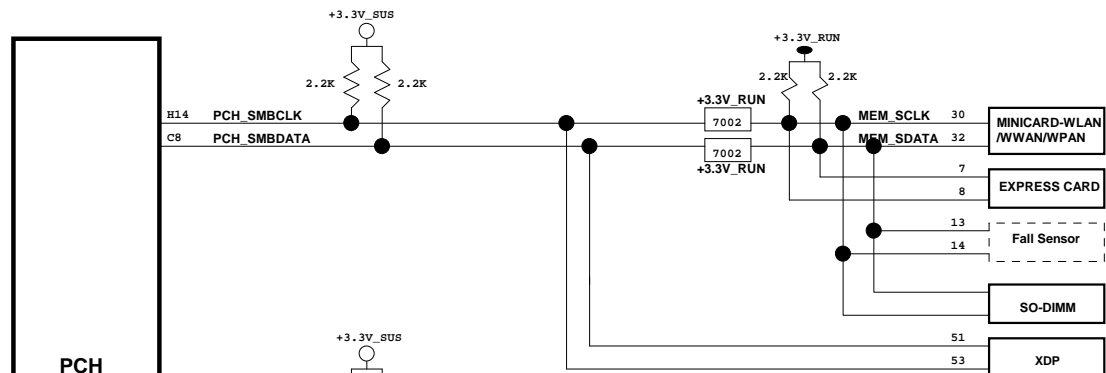
www.aitech1.ru

DEL PCH XDP as FM9 confirmed with Intel that its not necessary!

# RM5 Power Design Block Diagram 2009/02/25



- (1) AC : DC\_IN -> DC\_IN\_SS -> +PWR\_SRC
- Bat : +VCHGR -> +PWR\_SRC
- (2) +5V\_ALW2, +3.3V\_ALW
- (3) MAIN\_PWR\_SW#
- (4) 5V\_ALW\_ON
- (5) +5V\_ALW -> +15V\_ALW
- (6) SUS\_ON
- (7) All SUS power & PWRGD
- (8) SIO\_PWRBTN#, PCH\_RSMRST#
- (9) SIO\_SLP\_S5#, SIO\_SLP\_S3#
- (10) RUN\_ON\_1, RUN\_ON, GFX\_RUN\_ON
- (11) All RUN power & PWRGD
- (12) HWPG
- (13) IMVP\_VR\_ON
- (14) IMVP\_PWRGD
- (15) CLK\_PWRGD
- (16) RESET\_OUT#
- (17) PCH\_PWRGD
- (18) H\_CPUPWRGD
- (19) PLTRST#



www.aitech1.ru

POWER STATES

State \ Signal	SLP_S3#	SLP_S4#	SLP_S5#	S4_STATE#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	N/A	HIGH	N/A	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF	LOW	N/A	HIGH	N/A	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	N/A	HIGH	N/A	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	N/A	LOW	N/A	ON	OFF	OFF	OFF

PM TABLE

power plane \ State	+RTC_CELL	+DC_IN +DC_IN_SS +PWR_SRC +CPU_PWR_SRC +5V_ALW2 +MMB_PWR +3.3V_ALW	+5V_ALW +15V_ALW +5V_SUS +3.3V_SUS +3.3V_LAN +3.3V_CARDAUX +1.8V_SUS +1.5V_SUS	+VCC_CORE +0.75V_DDR_VTT +1.05V_PCH +1.1V_GFX_PCIE +1.2V_LOM +1.5V_RUN +1.5V_CARD +1.8V_RUN +3.3V_RUN +3.3V_DELAY +3.3V_R5C833	+3.3V_RUN_CARD +3.3V_CARD +5V_RUN +LCDVCC +5V_HDD +5V_MOD +5V_SPK_AMP +VDDA +GFX_PWR_SRC
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	OFF	OFF
S5 & S4 with AC or BAT	ON	ON	OFF	OFF	OFF
no AC/Battery	ON	OFF	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
NONE			

PCH IBEX PEAK-M	USB PORT#	DESTINATION
	0	Side pair Top / left
	1	Side pair Bottom / left
	2	USB W/ E-SATA port
	3	Reserved
	4	Mini Card (WLAN)
	5	Mini Card (WWAN)
	6	Reserved
	7	Reserved
	8	Mini Card (WPAN)
	9	TV
	10	Express Card
	11	Camera
PCH IBEX PEAK-M	PCI EXPRESS	DESTINATION
	Lane 1	Mini Card-1 WWAN
	Lane 2	Mini Card-2 WLAN
	Lane 3	Mini Card-3 WPAN
	Lane 4	Express Card
	Lane 5	Cardreader
	Lane 6	LOM